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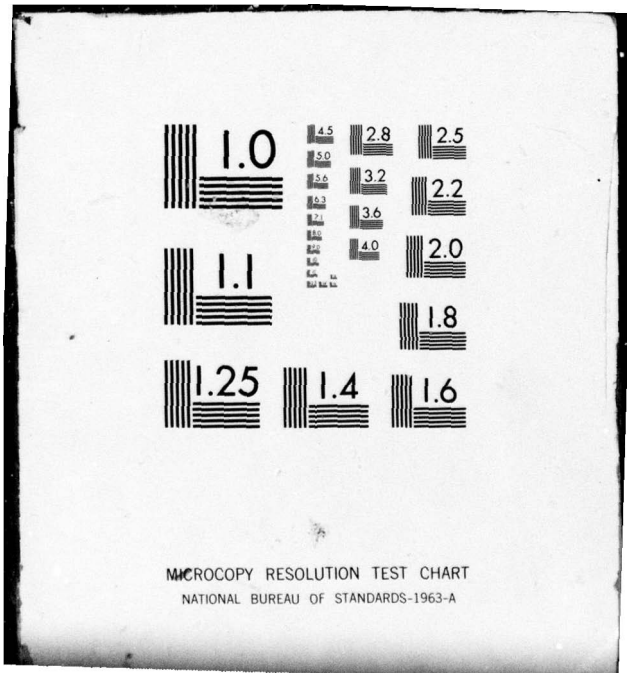
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RADC-TR-79-327
Final Technical Report
January 1980

AN OBJECTIVE PRINTED CIRCUIT BOARD TESTABILITY DESIGN GUIDE AND RATING SYSTEM

Grumman Aerospace Corporation

W. M. Consolla
F. G. Danner

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This final technical report presents the results of a study conducted by the Grumman Aerospace Corporation. The Project Engineer for Grumman Aerospace Corporation was Mr. Walter Monsen. The principal investigators were Mr. Fred Danner for the development of the testability guide and Mr. Wayne Consolla for the development of the demonstration procedure.

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-79-327 has been reviewed and is approved for publication.

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A methodology was developed during this study that a[illegible]tely evaluates the testability merits of a printed circuit board (PCB). This is accomplished through a "Figure of Merit" rating system that weighs the "difficult to test" and "easy to test" aspects of a circuit design.

The principal output of this study is an extensive Testability Design Guide that describes how testability problems associated with circuit structure

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can be corrected. The Design Guide works hand-in-hand with the rating system, such that the rating system identifies the nature and extent of the current testability problem and the guide provides the means to correct the design deficiencies.

The developed guide and evaluation procedures were demonstrated on a number of "difficult to test" PCBs which resulted in much improved fault isolation and significantly reduced test times.

ABSTRACT

The prime purpose of the study was to develop a Testability Design Guide showing how to correct PCB testability problems. Design considerations associated with circuit structure, initialization of sequential circuits, high ambiguity groups, clock line problem, feedback loops, "buried logic," and compatibility with Automatic Test Generators (ATG) are covered in the design guide. Once an evaluation of the circuit testability is made, the guide can be used to correct poor design features of the PCB.

Use of the PCB Testability Design Guide was demonstrated with a PCB design from the B-1 aircraft program. An initial testability evaluation rated this circuit as the most difficult to test of 28 PCBS reviewed. After testability modifications by methods presented in the Guide, the circuit was re-evaluated as "medium easy" to test. Laboratory results from tests on the AN/USM -429 Automatic Test Station (see figure 1) confirmed this improvement. All faults inserted were detected by the testable version of the PCB, and fault isolation was improved with reduced test times.

The second output of this study was development of a PCB Testability Evaluation System which will determine how testable a PCB is prior to release of the circuit to production, and which pinpoints the "bad design" features of the PCB. Corrections of these undesirable design features can then be accomplished using techniques found in the Testability Design Guide.

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Figure 1 Typical Integration of a PCB on the AN/USM-429 Test Station

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CONTENTS (contd)

ILLUSTRATIONS

ILLUSTRATIONS (contd)

ILLUSTRATIONS (contd)

EVALUATION

1. The objective of this study was to develop a design trade-off procedure that would enable logic board designers to determine cost-effective design considerations for printed circuit boards (PCBs) and to provide test engineers and maintenance personnel with fast, efficient and lower cost methods for PCB testing, and improved testability which should result in lower test programming and interface design costs.

2. A methodology that provides a means to determine and improve the testability of a PCB design has been developed. This technique is supported by a guide which describes various testability design techniques, and how these techniques can be used to redesign circuit areas that are difficult to test. Various weighting factors associated with both negative and positive design techniques are described in detail and methods by which a "figure of merit" of the testability design of a PCB can be determined is included. Other considerations of the study included the determination of the phases of system development in which testability design improvements should be incorporated and the management and system factors that could induce or encourage testability into a design.

3. The established guide and evaluation system was tested on 17 PCB samples and the results were compared against experienced engineering judgement. The results indicated that a high degree of correlation

existed between the testability evaluation technique and experienced engineer's judgement.

4. Further studies are recommended in testability design areas that include the further validation of the techniques developed in the study, and means to determine testability figures of merit from the microprocessor level up through to the system level.

5. The results of this study will be used as part of the upcoming "Testability Notebook" and to provide design engineers and program managers with the design tools and considerations in determining an effective testability design that can enhance the effectiveness of built-in-test (BIT) and decrease the high costs of supporting test systems.

James Saporito

JAMES SAPORITO
Project Engineer

1 - INTRODUCTION

The subject of testability for electronic circuits has recently been receiving major interest from industry and the DoD. Effective design for testability is essential in producing electronic systems maintainable within reasonable economic limits.

Effective design for testability can only be achieved if and when three fundamental conditions are met:

- Techniques must be employed to correct testability design problems at the earliest possible stage of development
- A "figure-of-merit" evaluation is needed to determine how much testability redesign is necessary to reach specified fault detection and isolation levels
- Program managements must be given financial incentives to achieve testability goals and to prevent high pressure "sell it off any way you can" deliveries which block implementation of meaningful design-for-test features.

This report emphasizes what should be done at the PCB circuit level to correct a design and make it testable. A Testability Evaluation Rating System was developed together with a comprehensive Testability Design Guide showing how to make specific design improvements.

Extensive reviews of literature, MIL-STDs and conference procedures led to the conclusion that an overall method to implement good testability at the circuit level did not exist.

With the need for a testability design methodology, three possible approaches to its implementation are:

- Complete testability evaluation and hardware changes prior to production release of a circuit design

- Discover the design weak points during test program integration, then incorporate production changes prior to field deployment
- Wait until a PCB is in the field and then perform statistical testability evaluations. Corrections to the design would depend on field test problems.

The first of the above approaches is the most desirable because corrections are easier and less expensive to make. However, there is a problem in achieving good testability earlier in the design phase since some of the more sophisticated traps to testing are difficult to detect prior to any attempt at actual modeling and software fault simulation. The Guide presented in this report is set up to provide maximum advance testability information about a circuit with the constraint that the testability evaluation and correction process should not take longer than 8 to 10 manhours. The data from circuit testability evaluations performed during the study show good correlation with actual "difficulty-to-test" information for a group of 17 sample PCBs. In all cases, the evaluation and the actual difficulty-to-test were within one grade of each other within the rating system.

Initial efforts to establish which material should be included as part of the Guide proved difficult because most published information used only a few obvious cases to prove the need for testability redesign. During the course of the study, specific redesign examples were collected and significant new factors were discovered.

Selection of the PCB from the B-1 aircraft program, as a testability demonstration circuit, caused considerable extra effort not originally anticipated. Analysis of this circuit showed that the PCB seemed to be deliberately designed to prevent successful automatic test generation of digital patterns. This difficult circuit design was advantageous in pinpointing many subtle testability design problems and contributed to a more comprehensive Guide.

The report is divided into the following major sections:

- Introduction - Section 1
- Survey of Testability Design Practices and Guidelines - Section 2
- Development of the PCB Testability Evaluation System - Section 3

- Testability Design Guide for Printed Circuit Boards - Section 4
- Cost Effectiveness Consideration - Section 5
- Testability Demonstration - Section 6.

2 - SURVEY OF TESTABILITY DESIGN PRACTICES & GUIDELINES

2.1 LITERATURE SURVEY

At the start of the study contract, a thorough review of available literature relating to testability of PCB electronics was made with emphasis on what possible factors really influenced how testable a circuit is, and, how will testability of PCBs be affected in the near future by introduction of new complex parts such as microprocessors, bubble memories, VLSI, etc.? Literature on the following subjects was included in this survey:

- ATE Equipment Design
- Automatic Test Generation Data Processing
- BIT Tradeoffs
- Bubble and Ultraviolet Erasable Memories
- Cost Tradeoffs for Testability
- Design for Testability
- Fault Diagnosis and Isolation
- Initialization of Sequential Circuits
- LSI/VLSI Testing
- Maintainability Considerations
- Microprocessors
- Placement of Test Points
- System/Management Factors
- Testability Specifications.

A bibliography of the literature reviewed during the study is included on pages 93 through 97 of this report.

While there are many documents and specifications with information on how to

make digital circuits more testable, no one single publication contained a realistic comprehensive method to accomplish this. Most literature described certain individual test factors with descriptive material on why they were important. Some reports showed mathematical approaches to guarantee PCB testability, but developed control systems to implement corrections after the hardware was in production. This would be cost and time prohibitive for most applications.

2.1.1 Significant MIL Standards

2.1.1.1 MIL-STD-415D (USAF, 8 Oct. 1971): Design Criteria for Test Provisions for Electronic Systems & Associated Equipment - The principal aim of this specification is to require adequate test points, BIT and self-check, and an external receptacle to connect ATE equipment. Guidance meetings and data requirements are employed to ensure compliance.

This spec only presents a fundamental control to see that the parties involved are conscious of the need for adequate test points, BIT, etc. It makes no attempt to guide a designer with specific instructions for building in circuit testability.

2.1.1.2 MIL-STD-1326 (U.S. Navy, 15 Jan. 1968): Test Points, Test Point Selection & Interface Requirements for Equipments Monitored by Shipboard On-Line Automatic Test Equipment - This standard establishes the requirements for providing ATE test points in prime equipments. It also provides criteria for optimum test point selection. These criteria are too general and all-inclusive to aid in resolving the testability design problem. The prime concern of this document is to place objective criteria on ATE signal interface characteristics of the unit under test (UUT).

2.1.1.3 MIL-STD-1519 (USAF, 17 Sept. 1971): Test Requirements Document, Preparation of - This standard sets requirements for the preparation and control of the Test Requirements Document (TRD) used to specify baseline data for electronic UUTs.

The document calls for the delivery of the schematics, logic diagrams, outline drawings, PCB connections, and other necessary data. It prescribes diagnostic flow charts and input/output (I/O) pin list information useful to a testability analysis. The "Family Tree" part number (P/N) information permits quick

access to required drawings, which overcomes a significant deficiency of related prints, i.e., failure to list next higher and lower assembly information.

This standard makes a valuable contribution to improved testability by forcing the designer to deliver a good set of documentation to the test engineer. It was written with the intention, however, of defining the PCB or module configuration. Other standards are necessary to define how testable the PCB is and how the design should be corrected for test purposes.

2.1.1.4 MIL-STD-2076 (AS) (1 Mar. 1978): Unit Under Test Compatibility With Automatic Test Equipment, General Requirements for - This specification is a later version of AR-8, the standard originally used to make equipments compatible with the VAST test station. It covers a large area of technology relative to the interface of the UUT with an automatic test station. Appendix B of this standard contains a check list for testability which gives considerable insight towards what is required to correct a design.

This document was an excellent attempt to control design of electronic modules and make them ATE compatible. It has tried to do too much however, and as a result, doesn't quite resolve the testability design problem.

The check list is not sufficiently objective; using evaluation words like "some", many, most, etc." when scoring testability factors. Further, each factor is weighed evenly and not relative to its importance. It is very expensive to fully comply with the myriad of requirements of this document. In order to satisfy many of the provisions, a designer's knowledge of the UUT or ATE is needed. This kind of information is not readily available and expensive to compile. The standard is important, and has led on this study to the concept of an improved PCB testability evaluation system capable of accurate prediction.

2.1.2.5 MIL-STD-2077 (AS) (9 Mar. 1978): General Requirements for Test Program Sets - This standard establishes requirements for development, test documentation, configuration management, quality control, and preparation for delivery of test program sets. It also shows certain testability information in a form of "things not to do" when developing and integrating a test program set. These restrictive testability factors were useful to the study.

2.1.1.6 MIL-STD-2084 (AS) (Preliminary): General Requirements for Maintainability of Avionics Equipment and Systems (will supersede AR-10) - This specification ties together all aspects of the maintainability process for avionic systems. Although it does not specifically deal with testability, it defines testability as the "characteristic of a design which allows the status (operable or inoperable) of a system or any of its subsystems to be confidently determined in a timely fashion." It calls for incorporating design features into the avionics to allow observability and controllability in the interest of test and maintenance.

2.1.2 Significant Literature

An extensive literature search was conducted to locate the latest information on both testability and on test techniques for microprocessors, bubble memories, VLSI, etc.

None of the literature presented a cohesive overall system for controlling PCB testability. Few papers tried to cover the testability task from the user's point of view.

In this phase of the study it became apparent that microprocessor manufacturers are not at present properly documenting internal logic design (see Figure 2-1). Without this detailed information the test engineer cannot model microprocessor logic.

One of our principal objectives during the survey was to extract potential testability rating factors or methods of correcting a design to make it more testable. Over 50 such testability factors were compiled and examined to see if they were significant enough for inclusion in the Evaluation System. Factors, which at the start of the program were considered basic and essential, were later discarded when found not to really affect the test development effort. The literature was valuable in suggesting ideas and stimulating thinking relative to new concepts for testability.

While many papers, reports and specifications containing information on testability were reviewed, five of these references provided significant insight to key aspects of the overall testability problem. These documents contributed in several ways to the formation of the present PCB Testability Evaluation System.

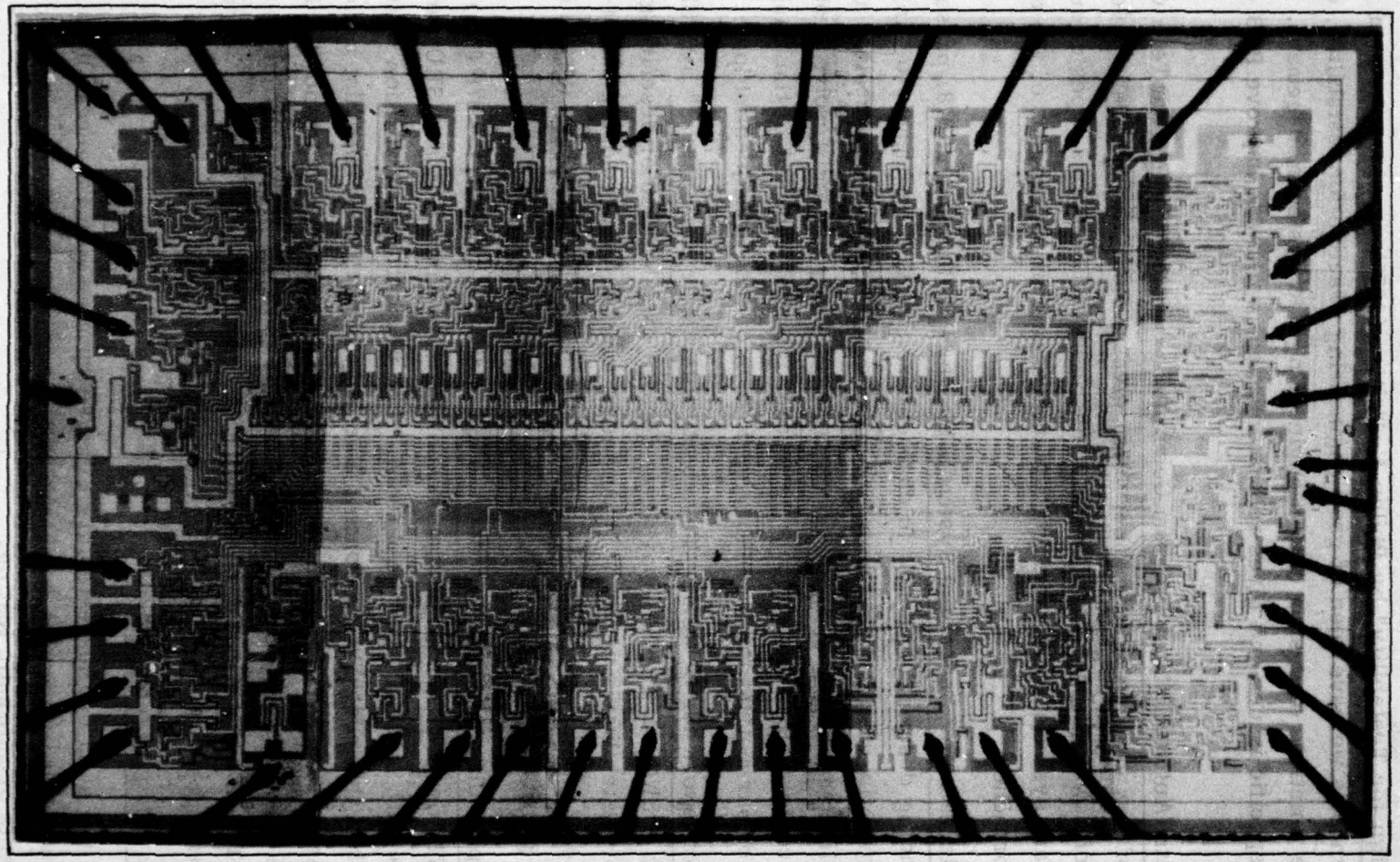

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Figure 2-1 Complex Microprocessor

—Internal Topography of a Typical Microprocessor Used in Today's PCB Circuits

"Design for Testability" by Phillip L. Writter (1975) provides the best condensed synopsis we have seen of good engineering practice for testability, combining the functions of system design engineering and system management. It examines specific issues and gives recommendations on how to improve PCB designs.

"Digital Automatic Test Program Generators - (PMS 306)" by ManTech Corporation of New Jersey (30 September 1978) gives a clear and comprehensive description of how ATG processing works, and reviews the various types of autotest software systems available citing advantages and disadvantages of the different approaches.

"Initialization of Sequential Systems" by Dr. Fuh-lin Wang (1978) presents an outstanding description of how to characterize the ATG problem in testing buried sequential circuitry and counters. Basic principles of initialization are covered with techniques to improve back-tracing of circuits and resolve problems with contradictory assignments of primary inputs. This led to the final definition of our method for testability evaluation of buried sequential logic.

"A Framework for Designing Testability into Electronic Systems" by William L. Keiner (NSWC/DL TR-3826 May 1978) does an excellent job of describing why design for testability is needed. It outlines a method for developing a testability specification but stops short of achieving specific testability design criteria and goals.

"Compatibility Task Scoring Data" - Appendix B - (MIL-STD-2076 (AS) 1 March 1978) develops a checklist approach to insure that LRUs and SRUs are compatible with automatic test equipment. The present PCB Evaluation System evolved from this checklist approach. The compatibility task checklist could not be used as written because of the subjective nature of several questions. The 4, 3, 2, 1 point system did not give an accurate determination of difficulty to test a UUT. In spite of its shortcomings, this document represents a very important attempt to improve the testability of circuit designs.

2.2 RELATED FIELD TRIPS

Since the start of the Testability Study, Grumman ATE Engineers have been active in several conferences, seminars and symposiums involving latest industry developments of automatic testing.

At the AUTO TEST EXPOSITION - (Boston, Mass. - Sept. 1978) Grumman presented a paper: "High-Performance Universal Switching System." Other papers of significance were presented on "Design for Testability on Analog Circuit Boards" and "Automatic Generation of Fault Isolation Tests for Analog Circuit Boards." The conference was held over a three-day period with technical sessions each day.

The Semiconductor Test Symposium - (Cherry Hill, N.J. - Oct. 1978) was more specialized with emphasis on Complex LSI Component and Board Design. Testability factors were highlighted in two of the technical sessions; one covering testability of components, and the other on testability at the board level. The emphasis of the latter session was on how to partition designs and selectively control functions to permit testing.

At the AUTOTESTCON '78 (San Diego, Calif. - Nov. 1978) papers covered both the hardware and software aspects of automatic testing, and for the most part were commercial and military status reports on major products. Grumman presented a paper entitled: "Design of a Functional Test Generator with a Functional Simulator for Digital Systems" which described recent development of the LOGOS III Automatic Diagnostic System. This paper was judged the outstanding paper given in the area of techniques for ATE.

In connection with the International Symposium on ATE - Brussels, Belgium, special technical sessions were conducted at Plessey Corp., London, England, in which Grumman presented details of the LOGOS III System development.

The ATE Seminar and Exhibit - (Los Angeles, Calif. - Jan. 1979) presented discussions on ATG vs. ITG (Automatic Test Generation vs. Interactive Test Generation). The discussion included the merits of processing all test patterns automatically versus using manual ATG patterns scored by machine. The topic "Is Simulation Dead?", covering new developments and the impact on simulation modeling was also covered.

Discussions with those attending these conferences and review of available technical papers and proceedings have contributed to development of the PCB Testability Evaluation System for this study.

2.3 INTERVIEWS WITH TEST ENGINEERS

During the initial phase of the study, interviews were conducted with twelve engineers who are engaged in automatic test design and integration. Their reactions and comments on the initial and revised PCB Testability Evaluation Systems were recorded. Some of the more significant comments are summarized in the following paragraphs. Revisions and improvements to the evaluation system resulted from many of these interviews which led to the final PCB Testability Evaluation System.

Most of those interviewed felt that the percentages of nodes accessible and the fan-out per wire-set factors were the most important of those listed. They generally agreed with the concept of an objective evaluation system, although several engineers questioned the validity of using a complexity part count. The complexity count factor was later modified because it was determined that there was very little correlation of test difficulty with the number of combinational circuits -- only with sequential portions of the PCB.

There was a consensus on the usefulness of factors which relate to specific test stations (No. of I/O pins, No. of power supplies, etc.); however, it was determined that there was no way to impose general ratings for these factors without knowing what test station would be used. Therefore, only specific data representing information about the PCB can be used for the rating evaluation.

Several of those interviewed expressed the need for better documentation. They indicated that poor documentation cost significant additional time for them to complete a test program set (TPS). Many examples of poor documentation were discussed. One engineer suggested that the design engineer be required to model the developed circuit in the format used to automatically process the test program. A tape should be delivered to eliminate translational errors when listing I/O pin designations, etc. Comments such as these led to the documentation evaluation factors of the final scoring system.

A clearer definition of how to assess the importance of proper initialization of sequential circuits was obtained in one interview. The need to be able to set a known logic state of a sequential circuit by both direct set and pattern input

set was realized. This is required by the test program so that a stage can be initialized when a test for a simulated fault is inserted. The PCB Testability Evaluation System was modified to reflect this concept.

A discussion with Grumman ATG experts led to a realization that the ratio of sequential to combinational circuits in a PCB was an extremely important concept which later correlation studies were able to substantiate. Initial scaling of this consideration was based on an 80% sequential circuit worst case (very hard) limit. Later study found that the PCBs became very hard to test when 50% or more of total circuit stages were sequential.

Some useful feedback was obtained from the interviews on where to find and obtain practical cost saving information. Costs-to-develop factors for PCB testing were detailed and areas for reduction of overall cost were highlighted. It was found that no current industry system for financial accounting of project expenses would give a breakdown of PCB cost-to-test factors. Use of a common interface device (ID) helps to lower costs. Surprisingly high costs are experienced in the areas of documentation and sell-off of PCB test program sets.

Need for the ability to remove a microprocessor (or VLSI) part easily from a PCB was stressed as a means of preventing excess testing costs. In digital circuits, the presence of an inaccessible clock is considered intolerable and stiff penalties are needed to force circuit redesigns. Similar penalties for use of high power or high voltage in a PCB were recommended by the test engineers.

The general reaction to the objective testability evaluation concept was very positive. Most people interviewed felt that the technical approach was sound and would lead to a significant test program cost reduction.

3 - DEVELOPMENT OF THE PCB TESTABILITY EVALUATION SYSTEM

At the beginning of this study an attempt was made to collect a list of all significant technical factors which might affect the testability of a PCB or module. A partial list of these factors is shown in Figure 3-1. Examination of several circuits and discussions on the merits and importance of these factors led to a preliminary method for classification.

Testability factors were separated into three (3) different classes:

- Basic Factors - Features which increased the complexity of testing in proportion to an increase in their number and are common to most PCB circuits
- Positive Adjustment Factors - Factors which tend to make a PCB become more testable
- Negative Adjustment Factors - Factors which reflect bad testability design, and increase the overall difficulty of PCB testing.

A decision had to be made on how best to proceed with the study. The alternatives were narrowed down to two principal approaches:

- Testability factors could be incorporated into an objective rating system with weighted scoring to determine PCB testability
- Full technical efforts could be expended into developing a case study type cook book as a guide in redesign for testability.

Motivation for pursuing the first approach came from review of Appendix B of MIL-STD-1276. There was a real question as to whether a rating approach could ever be made practical and objective. The feeling was that an objective evaluation system was possible and practical if enough depth could be achieved in the study. It would be necessary to determine the true conditions which affect the ability to test, and the relative importance to be attached to each of

1 – Unusual Discrete Components
2 – Use of Clocks: Inaccessible, Free Running, Override, Externally Disabled, Critical Frequency
3 – Keyed Pins on Connector (Defeatable)
4 – Number of Different Logic Families
5 – Supply Voltage(s): Sequencing Necessary, Number of Different Voltages, Polarity, Floating Ground
6 – Non-Standard Parts or ICs (Impact on Modeling)
7 – Test Points: Also Control Points, on Connector or Individual
8 – Connector(s) – Number of Pins
9 – Special High Power Needed
10 – High Frequency Needed
11 – Difficulty to Initialize Sequential Ckts – Direct, Indirect
12 – Memory on Card, Prgrammable
13 – Sockets for ICs, Discretes
14 – Adjustments (Trimpots, etc.)
15 – Wired "ands" and "ors"
16 – Large or High Fan-In, Fan-Out Lines
17 – LEDS
18 – Functional Partitioning of Ckts
19 – PCB Signature Resistor to Stop Wrong Test
20 – Throw-Away or Repairable
21 – Component Reference Designations (Clear)
22 – Pull Up Resistors Required in ID
23 – Quality of Schematic Layout
24 – Availability of Spare Gates
25 – Reactive External Loads in ID
26 – "Domino" or Multiple Induced Failure Probability
27 – Fiber Optics
28 – Monostables – Buried, Monitor, Control Externally
29 – Power-Up Reset
30 – Buried Logic
31 – Fail Safe Design
32 – High Accuracy Measurements, Tight Tolerances, etc.
33 – Heat Sink Required, Cooling Air Required
34 – Non-Isolatable Gates in Parallel but Not in Same Package
35 – Warm-Up Time
36 – Power and Ground, Pins Standardized
37 – Self-Test Built-in
38 – Test Point Characteristics – Isolation, Protection
39 – Number of Total Circuit Nodes
40 – Number of Total Input Leads
41 – Number of Total Output Leads
42 – Long Counters – Buried, Monitor, External Control
43 – Number of Internal (Individual) Test Points
44 – Clock Phases Required – Total Number
45 – Uses Microprocessor, VLSI – Non-Removable
46 – Uses Memory Arrays – Multiple, Parallel Wired – Non-Removable
47 – Condition of Reset Line for Sequential Circuits
48 – Special External Loads Required
49 – Gate Per Package Isolation Factor
50 – Number of New Logic Block Models Needed
51 – Serial Strings of Logic Gates
52 – Total Complexity of PCB
53 – Operator Action Required
54 – Total Number of Packages/Parts
55 – Probe Access to PCB Packages/Parts
56 – Number of Different Logic Voltages

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Figure 3-1 Early List of Possible Testability Circuit Factors

these. This task was truly a research effort because there was no precedent for such objectives.

The second approach appeared plausible until the actual attempt was made to accomplish it. The literature contains numerous before and after illustrations of how to make a circuit more testable. However, all of the many examples reduce down to six or seven obvious redesign fixes. The authors all choose obvious cases to quickly convey ideas during technical presentations. Thus, there were only a few good examples which illustrated their points, leaving insufficient data for a cook-book approach to produce a good testability guide using known case studies.

As a result, there appeared no other technical choice than to develop a representative evaluation system as a first step to understanding design for testability. Once the evaluation scoring was proven accurate, it would be used on actual circuits to produce before and after examples of testability redesign.

3.1 DEVELOPMENT OF THE INITIAL TESTABILITY EVALUATION SYSTEM

As a first attempt to develop a testability evaluation system, 12 basic factors, 3 positive factors, and 20 negative factors were selected. Scale factors (score differences) were assigned with respect to expected worse case limits. Categories of the initial evaluation system are listed in Figure 3-2.

After evaluating several PCBs the scores were analyzed to determine if each factor was discriminating properly with respect to the actual degree of test difficulty. This initial evaluation system did not stand up to a critical review.

3.2 DEVELOPMENT OF THE REVISED EVALUATION SYSTEM

Several changes were incorporated to develop a revised evaluation system. The number of basic factors were reduced from 12 to 8. Additions to the positive and negative factors were made, and the scaling increments were revised for closer correlation. Interviews with test experts resulted in further revisions to the evaluation system.

BASIC FACTORS

1 – Number of Nodes
2 – Number of Parts
3 – Number of Nodes per Part
4 – Part Accessibility
5 – I/O Pins
6 – Nodes per I/O Pin
7 – Number of Logic Voltages
8 – Functional Modularity/Independence
9 – Number of Power Supplies
10 – Total Number of Wire Sets
11 – Normalized Weighted Number of Parts per Wire Set
12 – Percent of Wire Sets Accessible

POSITIVE FACTORS

1 – Sockets
2 – Uniform Pins
3 – Labeling

NEGATIVE TEST FACTORS

1 – Monostable
2 – Counters (Pkgs x Stages)
3 – Max. Number Parts per Wire Set
4 – Sequence Supply Voltages
5 – Non-Removable Memories
6 – Non-Removable Microprocessor
7 – No Reset Line
8 – External Loading Required
9 – New Logic Blocks
10 – Buried Sequential Logic
11 – Warm-Up Time
12 – Tolerance
13 – Non-Defeatable Keyed Pins
14 – High Power
15 – Frequency Critical
16 – No Signature Resistor
17 – Clock Lines
18 – External Test Equipment
19 – Environmental
20 – Adjustments

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Figure 3-2 Factors Used for the Initial Testability Evaluation System

Eight basic factors were selected:

- Complexity Count - The higher the complexity count, the more ATG patterns and simulated faults are required. Assignments were made with limits and increments tailored to worse case values. Difficulty to test is directly proportional to the complexity of the circuit
- Number of Function Blocks - This factor began as a simple count of the number of parts on a PCB. Problems arose with the accuracy of this factor because earlier discrete part circuits were penalized unjustly even though they were relatively easy to test. The part count approach was changed to a count of logic blocks where functional groups of discrete parts were counted as one "functional block." IC chips were still counted as one because breaking them into individual logic functions was too time-consuming to the evaluator and did not give much added refinement to the score. Non-functional parts such as pull-up resistors and filter capacitors are not counted
- Part Count Per Function Block - The more complex the internal structure of a part, the harder it is to test. This factor reflects how hard it is to test an average PCB part
- Number of I/O Pins - Originally, the increased number of I/O pins on a PCB was considered negatively. More tests would have to be generated and too many I/O pins might be difficult for ATE to handle. Extra switching would be necessary in the interface device (ID). After reassessment of typical PCBs it was decided that more I/O pins make it easier to test until a point is reached which exceeds the capability of the test station. Scoring was changed to reflect this change in concept.

  The question of whether to separate input and output pins in the scoring was also considered. It was decided not to take this extra step because it did not appear to change the scoring to any marked degree, and defining each individual pin would be too time-consuming for the evaluator

- I/O Pins per Function Block - This factor represents the internal accessibility of the test station to the parts on the PCB. It can easily be obtained from the number of I/O pins and functional blocks
- Total Number of Nodes - This factor reflects the fact that the greater the number of nodes the harder a PCB is to test
- Normalized Weighted Number of Function Blocks per Node - This factor represents the average fanout of internal and external node points of a circuit. The higher the average internal fanout, the more difficult fault isolation becomes
- Percent of Nodes Accessible - This was judged the most important individual factor in the evaluation system. Automatic test systems can logically deduce states of PCB gates to a high level when most of the nodes are brought out to I/O pins. In cases where a large number of nodes are inaccessible, the circuit becomes almost impossible to test.

  Inaccessible nodes which connect two points on the same package, or connect two different packages with one wire, are considered acceptable (no penalty to score) since they are in the simplest form possible. Three or more leads to the same IC package are counted as one and would not cause a penalty for inaccessibility unless the adjusted count is still greater than two.

Positive factors were those which would make the testing easier if they were present. Factors of this nature concern the physical qualities of the PCB packaging:

- Use of Sockets (if microprocessors, VLSI, etc.)
- Uniform Power Pins
- Proper Labeling
- Physical Access to PCB Parts
- Lack of Conformal Coating.

Credit was given for the presence of any of these factors including lack of conformal coating, which makes the PCB more testable.

Twenty-five negative factors which represent bad testability design practice were defined. These factors (shown in Figure 3-3) were selected to reveal bad design features and point directly at the area of the PCB where corrective measures should be taken.

Heavy penalties were given for such bad practices as failure to properly initialize sequential circuits and the presence of an uncontrollable, inaccessible clock circuit. This was intended to force correction of these critical PCB problems.

Many of the negative factors are set up to penalize the circuit for the number of times a bad design practice is used. Such penalties give a more realistic appraisal of how bad the design is.

The revised testability evaluation factors were much more closely aligned to the actual difficulty of test.

Following correlation testing using the revised system, each testability factor was carefully reviewed and rejustified. Surprisingly, after all the steps to define the basic factors, only two of the eight basic factors were judged very significant:

- Percent of Nodes Accessible
- Complexity Count.

The revised complexity count factor was misleading because combinational logic adds little to the overall difficulty to test. Automatic test generators will process large amounts of combinational logic with no problem and 100% of fault detection. This is possible because all logic states are known at all times. The complexity count factor was changed to count only sequential logic and to count combinational logic only when it was an internal part of a sequential IC chip.

Two new basic testability factors evolved from the revised evaluations. First, the percent of sequential circuits in the total mix of logic is directly proportional to test complexity. Second, proper documentation is of significant importance. The problems encountered with the documents supplied for the typical test job are monumental. Bad documentation causes a significant part of the overall test problem.

1 MONOSTABLE CKT – A one-shot which uses RC time constant for its pulse width.

2 COUNTERS – Count number of packages x number of internal stages. Penalty for each instance.

3 MAX NUMBER FUNCTION BLOCKS PER NODE (NO ACCESS) – Count number of different function blocks connected to same wiring junction.

4 MAX NUMBER FUNCTION BLOCKS PER NODE (ACCESSIBLE) – Count number of different function blocks connected to same wiring junction (node) where lead from this node reaches an I/O pin.

5 SEQUENCE SUPPLY VOLTAGE – Two or more supply voltages which require a turn-on or turn-off sequence.

6 NON-REMOVABLE MEMORIES – Any type of memory which is permanently wired or soldered to the PCB.

7 NON-REMOVABLE MICROPROCESSOR, VLSI – Any microprocessor, VLSI which is permanently wired or soldered to the PCB.

8 INITIALIZATION OF SEQUENTIAL CKTS – Flip-flops and other sequential Ckts should be resetable from an external connector pin (either set or reset) and by applying a digital stimulus of less than 16 patterns to the PCB. Penalties are assessed if either type of reset is absent, and severe penalty for no reset capability.

9 EXTERNAL LOADING REQUIRED – Components which must be added to the ID to perform test.

10 NUMBER OF DIFFERENT LOGIC TYPES – A logic type represents a logic block which must be modeled for ATG processing. Excess numbers of different types receive a penalty due to increased effort for the test engineer.

11 BURIED SEQUENTIAL LOGIC – Number of serially connected sequential logic stages isolated from I/O pins.

12 MAX NUMBER OF SERIAL GATES – (NO ACCESS) – Excessively long strings of serial gates without leads to the I/O pins cause difficulty with ATG fault isolation definition. Penalties are rated for each instance.

13 EXCESS WARM-UP TIME – Time required to stabilize card should not exceed 3 minutes.

14 TOLERANCE – Analog measurement tolerances tighter than those achievable with available test equipment.

15 NON-DEFEATABLE KEYED PINS – Keyed pins requiring a separate connector for each PCB.

16 HIGH POWER – High voltage (over 300V) or high current complicating the ID.

17 FREQUENCY CRITICAL – Frequency measurement more critical than those achievable with available instrumention.

18 CLOCK LINES – Any inaccessible clock in PCB circuit should be redesigned prior to test.

19 EXTERNAL TEST EQUIPMENT – Test equipment other than that contained in the automatic test equipment.

20 ENVIRONMENTAL – Special chambers or areas required to perform test.

21 ADJUSTMENTS – Trimpots, variable caps, etc.

22 COMPLEX SIGNAL INPUTS/OUTPUTS – Signals where interpretation by the test operator is required or where complex or non-periodic waveshapes are used.

23 REDUNDANT LOGIC – Logic which because of being in parallel prevents fault isolation (FI) of individual logic functions. No penalty if built-in-test permits FI of redundant elements.

24 NUMBER OF LOGIC VOLTAGES – Number of drive logic voltages which must be supplied by the tester.

25 NUMBER OF POWER SUPPLIES – Number of separate power supplies which must be supplied by the test station.

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Figure 3-3 Negative Factors for the Revised Evaluation System

3.3 DEVELOPMENT OF THE FINAL TESTABILITY EVALUATION SYSTEM

In the final system the positive factors were eliminated or transformed to equivalent negative factors.

Revisions to the negative factors were made for increased accuracy and to add five specific documentation factors. An analysis was performed to improve the assessment process for buried sequential logic. The technique used in the revised evaluation system was too difficult. It was replaced by a rating process where scores are based on clusters of buried sequentials which are connected through the signal leads or by a signal to clock lead combination. The new rating approach can be tabulated in a few minutes and gives reasonable representation of the extent to which buried circuitry will impact testing.

3.4 PCB CORRELATION STUDIES

The principal problem with previous approaches to the determination of PCB testability appears to be failure of the researchers to follow through and check to see if their concepts were workable. Proof of any evaluation scheme must demonstrate that the evaluation process is accurate and that the design corrective action is obvious and forced by the nature of the process being implemented.

Each time PCBs were scored to assess their relative testability, new and different discontinuities emerged and pointed to shortcomings in the evaluation factors. These apparent discrepancies were the key to an understanding of what makes a PCB really testable. Three revisions of the rating approach were made before the evaluation results tracked favorably with actual test experience. Objective PCB evaluations revealed difficulties with microprocessors, compilation of node counts, large memory chips, assessment of internal circuit accessibility, and complexity part count. The density of parts on a PCB was found to be constant for a wide range of hardware examined, so it was replaced by other mechanical/packaging accessibility considerations. A group of ten PCBs were then evaluated to establish whether the system did an effective job of predicting testability and whether the system would point out specific places where redesign was necessary. Figure 3-4 shows five of the PCBs. As this work was progressing, careful attention was given to the overall test philosophy of the

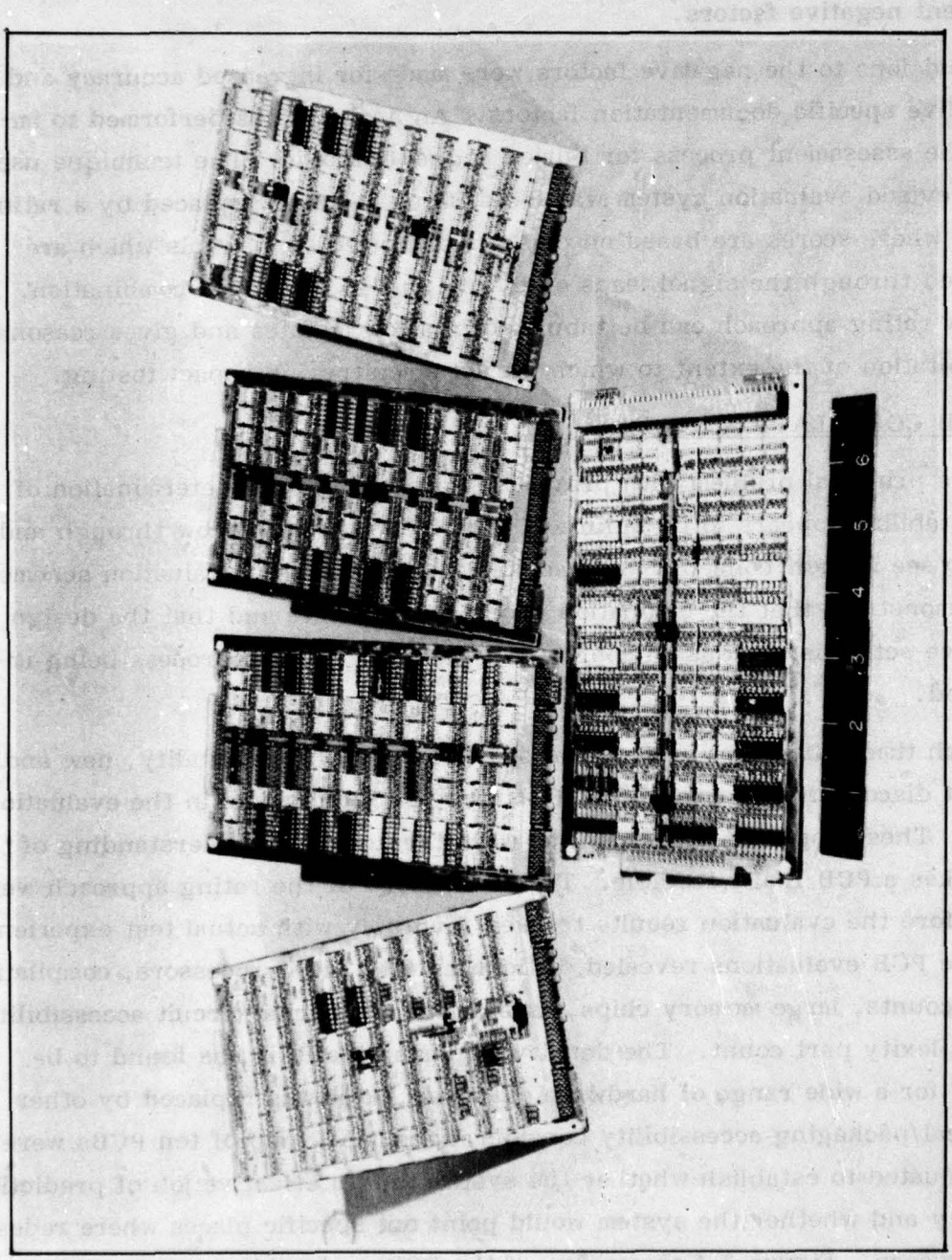

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Figure 3-4 Five of PCBs Evaluated

evaluation system, and to whether each individual factor was weighted correctly. Results showed that the penalty for increased I/O pins should actually be reversed since more access makes testing easier as long as the ATE limit is not exceeded. The idea of rating the functional modularity of a PCB was judged too subjective to be practical and consequently was abandoned. The percent of leads accessible factor was modified so as not to penalize the designer for inaccessible leads connecting less than three parts. More confidence was gained in the use of the testability evaluation system. The negative factor scores clearly indicated design features which had to be corrected, and the resulting quantitative testability gains.

A second group of 17 PCBs was selected for evaluation of the improved factors. Test engineers classified the real difficulty of testing each PCB and explained detailed problems they experienced which justify the ratings. One group of cards in the test sample had a range of difficulty from very easy to very hard which aided in confirming the accuracy of the rating.

As the study progressed it became obvious that poor documentation caused a severe cost penalty to test set development and field testing. Other not so obvious test factors were uncovered. The importance of PCB compatibility with automatic test generation (ATG) became more significant than expected and will become even more significant in future years.

It was further determined that positive factors, where bonus points were given for good testability features, were not significant enough to be retained because they did not show relative test difficulty. Another ATG related change was to consider only sequential circuits in rating complexity, and to add the ratio of sequential to combinational circuits as an important testability factor. Once automatic test generation is used as the standard method for developing test program sets, all logic states of combinational circuits can be easily tested. Only sequential circuits add to overall complexity.

Results of evaluating the 17 PCBs led to the final revision of the Testability Evaluation System using only basic and negative factors. The same 17 PCBs were used to see if close tracking of the ratings and the actual test engineer's evaluation would occur. Figure 3-5 shows detail results of the evaluation. There are only minor differences when comparing the scores derived from the Testability Evaluation System to the actual difficulty-to-test defined by the test engineers.

CARD P/N	TOTAL RATING SYSTEM SCORE (%)	ENGINEER'S RATING	TESTABILITY EVALUATION SYSTEM RATING*
8354291-501	56	Med-Easy	Med-Easy
8354321-504	75.8	Easy	Easy
A51S24156	29.2	Hard	Hard
A51S24162	35.1	Hard	Medium
60004	66.2	Med-Easy	Easy
60112	59.6	Med-Easy	Med-Easy
60001	5.8	Very Hard	Very Hard
A32S4010-1	-10.6	Very Hard	Very Hard
755-1405	46.6	Med	Med-Easy
20380	21.6	Easy	Med-Easy*
20510	40.7	Easy	Easy*
20500	33.7	Easy	Med-Easy*
20064	6.7	Very Hard	Medium*
20030	18.3	Medium	Med-Easy*
20320	4.4	Very Hard	Medium*
617454	-22.9	Very Hard	Very Hard
20310	7.2	Hard	Medium*

*Poor documentation was not reflected in evaluation by test engineers but did cause a large increase in cost to test. Documentation factor was removed to make a valid comparison. (Poor documentation factors lowered testability ratings by 30%)

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Figure 3-5 Results of Sample PCB Rating Study for Final PCB Testability Evaluation System

A high degree of confidence has been established in the validity of this testability rating approach because the engineers who performed the evaluation were the same engineers who actually prepared and integrated test programs for the PCBs.

4 - TESTABILITY DESIGN GUIDE FOR PRINTED CIRCUIT BOARDS

This testability design guide for printed circuit boards (PCBs) is written to assist the design engineer in properly designing a PCB for testing.

Subsection 4.1 of the guide presents examples of testability corrective methods and techniques which can be used to eliminate PCB test deficiencies.

Subsection 4.2 presents a checklist of system/management factors which are applicable to a group of PCBs or a system, and which may be related to specific ATE equipment.

Subsection 4.3 of the guide provides a PCB testability evaluation system which develops the "Figure-of-Merit" and identifies areas where design corrections are needed. A step-by-step description of how to perform a PCB evaluation is also provided.

4.1 DESIGN CORRECTIONS FOR GOOD TESTABILITY

This part of the guide presents specific methods and techniques for correcting hard-to-test designs. When maximum advantage is taken of these corrective measures, PCB testability will be improved to a point near its generic testable limit. In many digital circuits this may mean that all single point failures stuck at "1" or "0" can be detected and isolated to an ambiguity group of 4 or less replaceable parts. In some cases this ideal solution will not be possible, but in every case the circuit testability will be greatly enhanced.

4.1.1 Circuit Structure Factors

4.1.1.1 Initialization - Almost half of the design problems associated with use of sequential circuit stages on a PCB are caused by a failure to provide for proper circuit initialization.

The ability to set the logic state of a flip/flop to a known position is also required when simulating faults in one or more lines leading into the stage. It is therefore important to design the circuit so the sequential stage can be set

to a known state by both the set/reset inputs and by clocking. This permits the known logic state to be set when the simulated fault prevents the reset from occuring on the normal reset path. Leads should be connected to primary inputs and outputs when possible; the more this can be done, the better.

Typically, when there is no functional need for the set (S) and reset (R) inputs, good circuit design practice calls for the return of these leads to $+V_{CC}$ (see Figure 4-1).

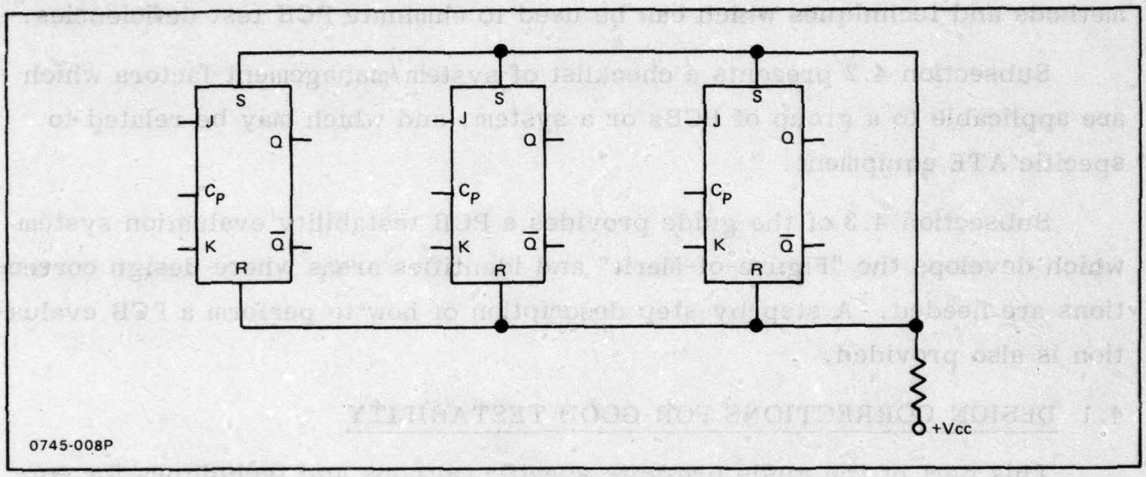


Figure 4-1 Poor Design of Flip/Flop Reset Lines

This is a poor design for testability because it denies the test engineer the use of the alternate reset approach for the JK flip/flop. A correct technique for proper return of the S and R input leads is shown in Figure 4-2. S could also have been brought out, or both S and R can be brought out.

By returning the R inputs to an external pin, the stages can be reset while the C_P fault is being simulated leading to a detection and isolation of this simulated fault. When the circuit is in the system, $+V_{CC}$ voltage can be applied to this external pin to fulfill the design functional requirement. Connecting more than four of the above stages together is not recommended, since this would create a high fan-out with ambiguity during the fault isolation portion of the test program.

Sequential stages can be initialized when power is first applied by using the network shown in Figure 4-3.

As $+V_{CC}$ is applied, the initial voltage across C is 0. After four constants (T = 4RC) voltage V_1 reaches $+V_{CC}$ which effectively removes the initialization network from affecting the flip/flop.

For cases where flip/flops are reset from an uncontrolled internal circuit point such as shown in Figure 4-4, the logic should be redesigned to permit the circuit configuration of Figure 4-5. This assumes the logic is designed to permit a state change from the primary input to reset the flip/flop.

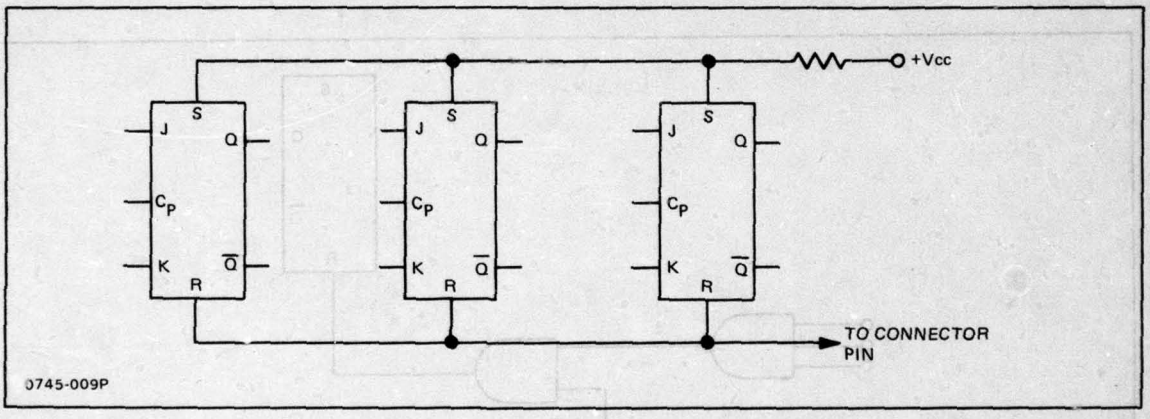


Figure 4-2 Good Testability Reset Design for Flip/Flop

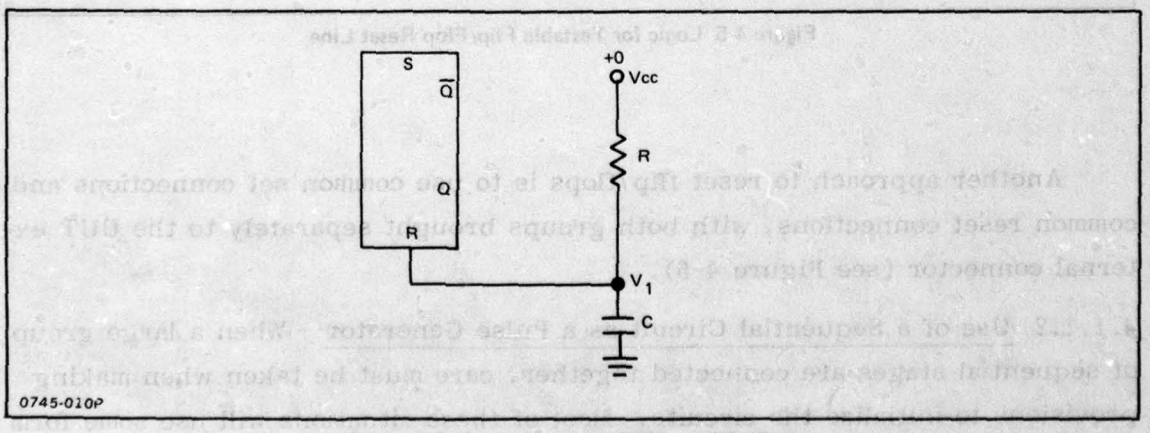


Figure 4-3 Technique to Initialize a Flip/Flop

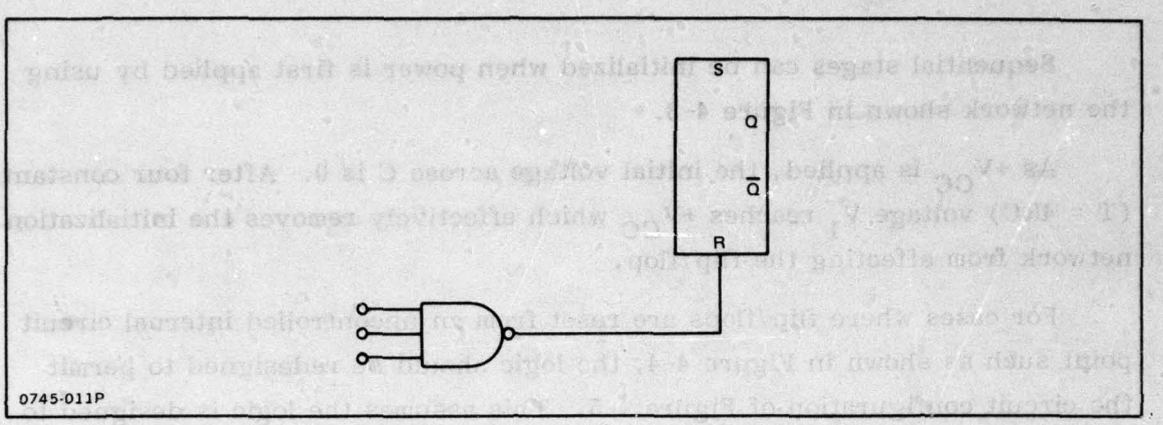


Figure 4-4 Uncontrolled Internal Flip/Flop Reset Line

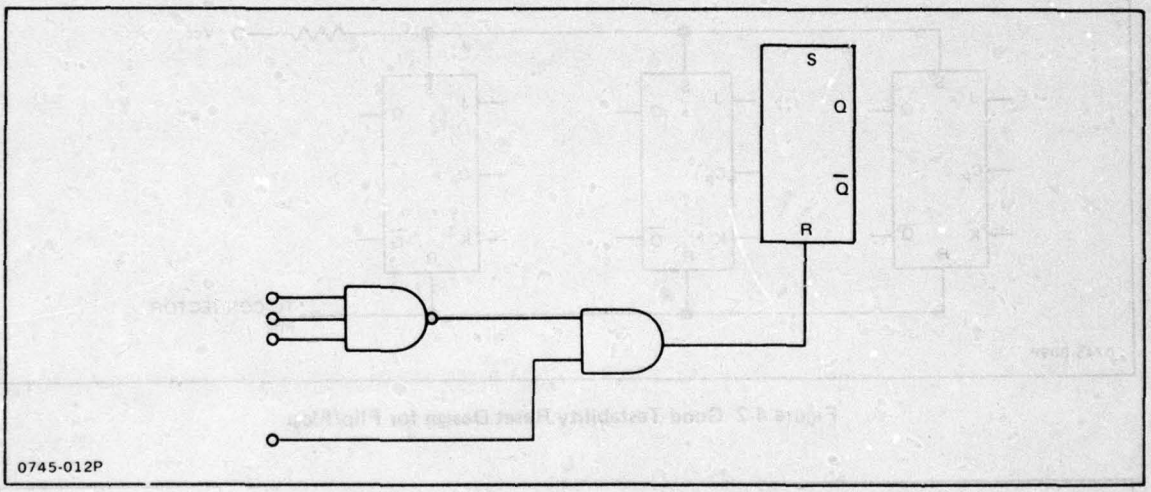


Figure 4-5 Logic for Testable Flip/Flop Reset Line

Another approach to reset flip/flops is to use common set connections and common reset connections, with both groups brought separately to the UUT external connector (see Figure 4-6).

4.1.1.2 Use of a Sequential Circuit as a Pulse Generator - When a large group of sequential stages are connected together, care must be taken when making provisions to initialize the circuits. Most of these situations will use some form of automatic test generation to form the test patterns used to stimulate the

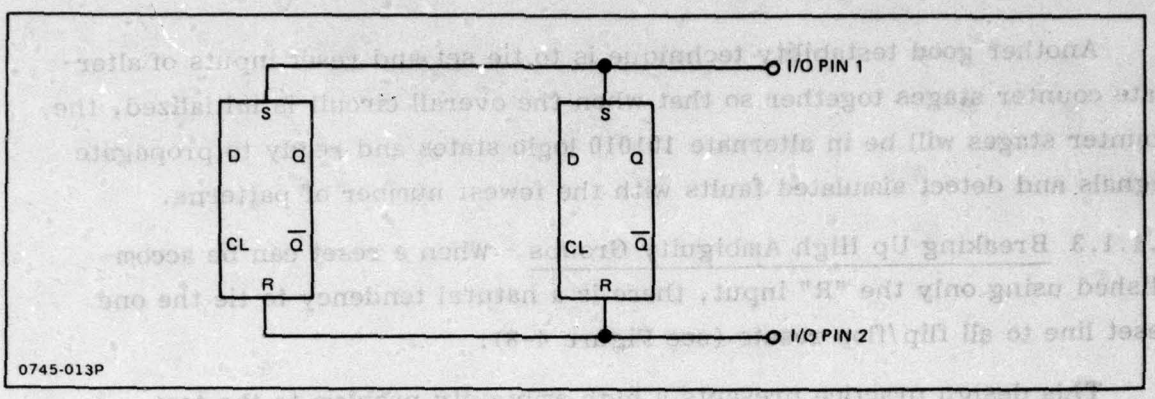


Figure 4-6 Use of Primary Inputs to Reset Flip/Flop

circuit. It is useful to set up a sequential stage in critical parts of the circuit as a pulse generator or "test clock". This is accomplished by returning the direct set and direct reset stage inputs to independently controlled leads which are primary circuit inputs (see Figure 4-7). The "test clock" stage can now be used to propagate a series of 10101010 logic states to the output.

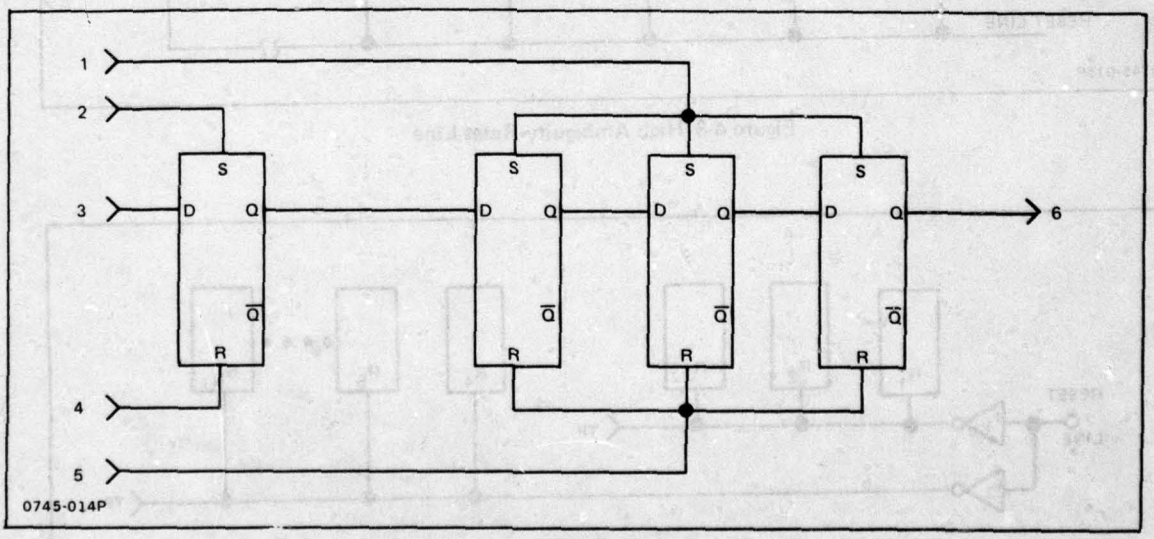


Figure 4-7 Use of External Control of Flip/Flop as Pulse Generator or "Test Clock"

Another good testability technique is to tie set and reset inputs of alternate counter stages together so that when the overall circuit is initialized, the counter stages will be in alternate 101010 logic states and ready to propagate signals and detect simulated faults with the fewest number of patterns.

4.1.1.3 Breaking Up High Ambiguity Groups - When a reset can be accomplished using only the "R" input, there is a natural tendency to tie the one reset line to all flip/flop resets (see Figure 4-8).

This design practice presents a high ambiguity problem to the test engineer. Reset lines of this type should be broken into groups, with the reset line buffered by logic into each group (see Figure 4-9).

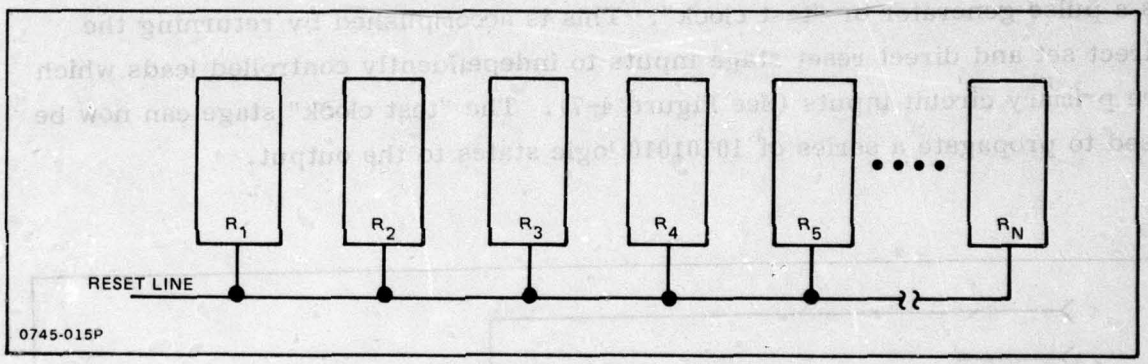


Figure 4-8 High Ambiguity Reset Line

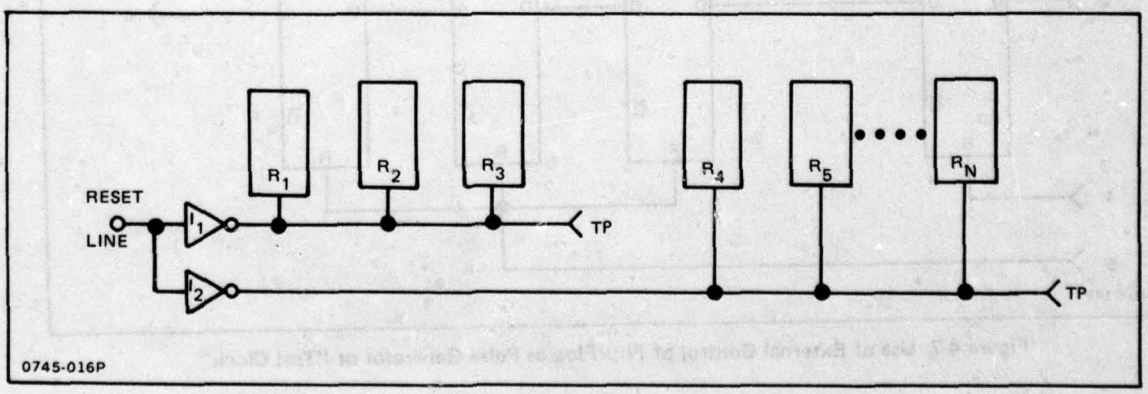


Figure 4-9 Design for Testability Break Up High Ambiguity Reset Line

Ambiguity of each node in the reset line is reduced by using this technique. If R_1, R_2, R_3 stages are all in different packages, a test point access lead should be added to improve the node testability. When possible, stages R_1 and R_2, or other pairs connected to the same reset branch, should be from the same IC package. This reduces ambiguity still further.

Groups of combinational gates should be from the same IC package (see Figure 4-10) whenever possible.

For redundant gates used to lower the drive impedance, all legs of the redundant circuit should be from the same circuit package (see Figure 4-11). If a redundant logic group is modeled for ATG processing and all parallel gates are from the same logic package the ATG model should show only a single gate instead of two or three. This eliminates race or non-detect problems with the data processing.

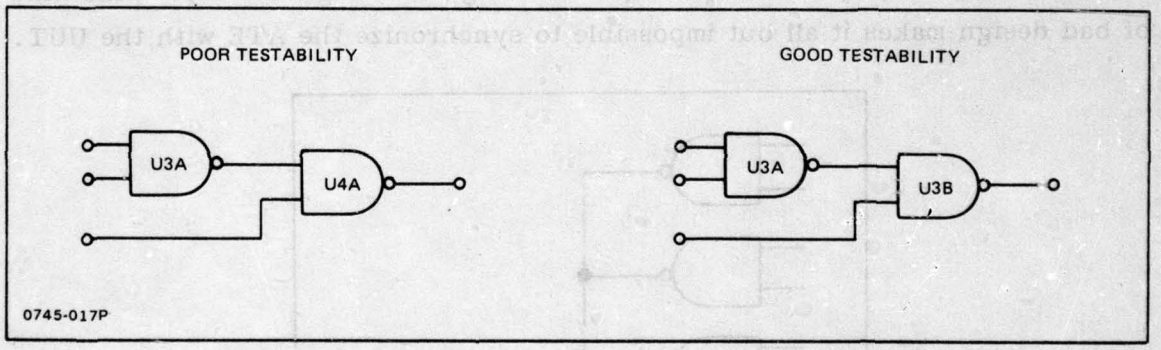


Figure 4-10 Use of Common IC Package for Related Gate Logic

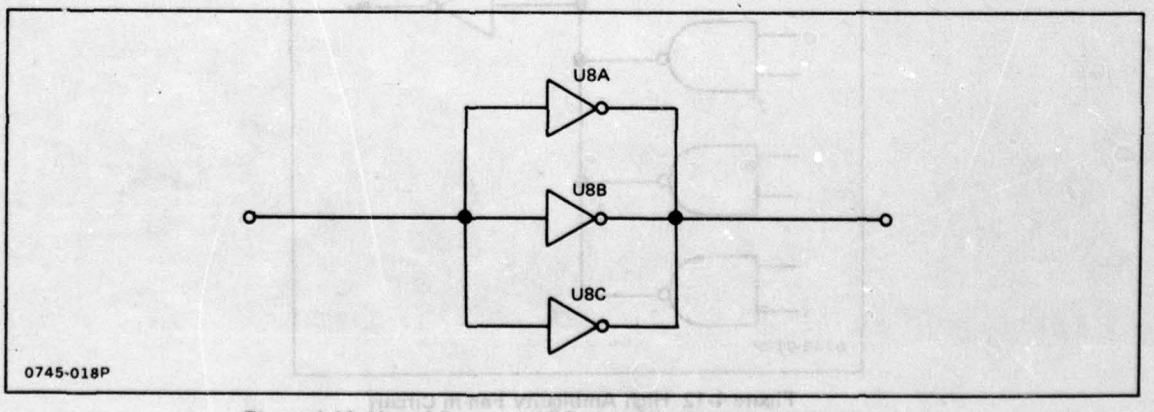


Figure 4-11 Use of Common IC Package for Redundant Gate Logic

When using wired NAND circuits break up high fan-in of outputs (Figure 4-12) by splitting into two or more branches with a maximum of three packages (inaccessible case) joined to a node or four packages if the node is connected to an external lead (see Figure 4-13).

Correspondingly, high fanouts require use of extra output stages (see Figure 4-14 and 4-15) to reduce fault ambiguity.

The impact of adding test leads to gain access to high ambiguity points in the circuit has a limited value. While it does improve testability somewhat, there is no substitute for dividing down fan-in and fan-out points to uniquely fault isolate the circuit nodes to an acceptable level.

4.1.1.4 Clock Line & Oscillator Problems - Circuits which contain continuously running oscillators, clocks, or pulse generators without access to external PCB inputs or outputs present an unacceptable design (see Figure 4-16). This kind of bad design makes it all but impossible to synchronize the ATE with the UUT.

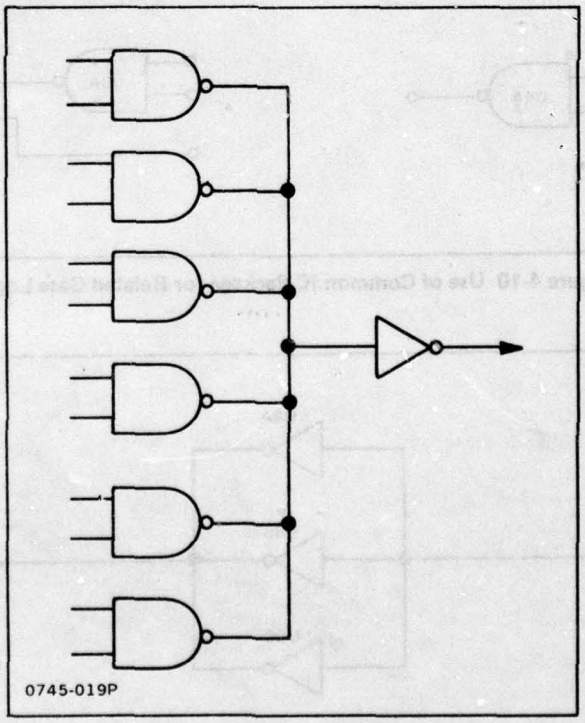


Figure 4-12 High Ambiguity Fan-in Circuit

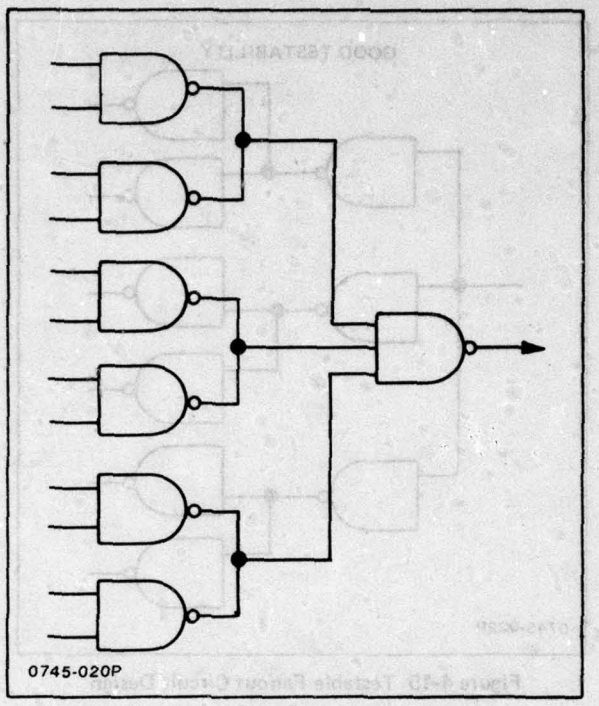


Figure 4-13 Testable Fan-in Circuit Design

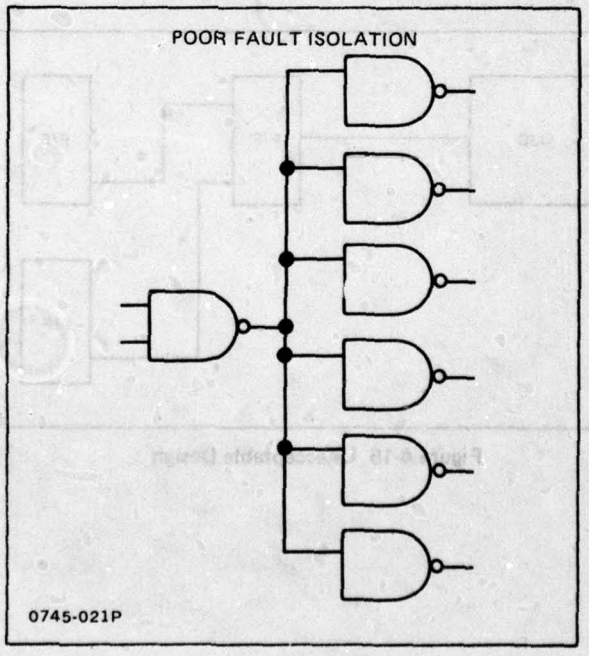


Figure 4-14 High Ambiguity Fanout Circuit

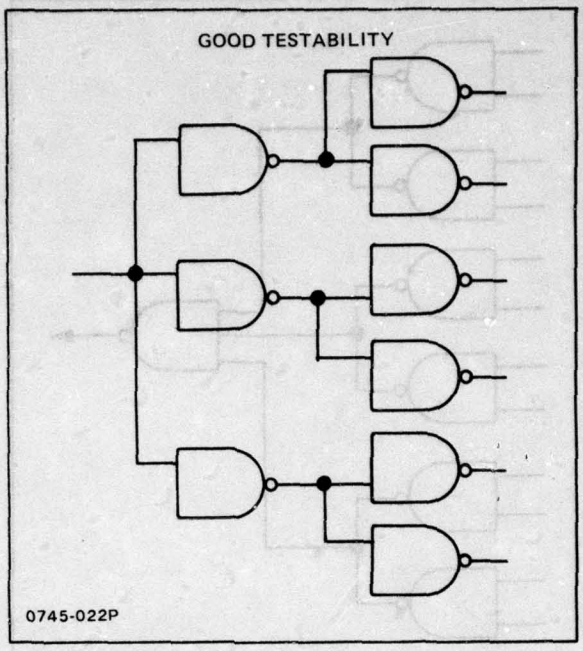


Figure 4-15 Testable Fanout Circuit Design

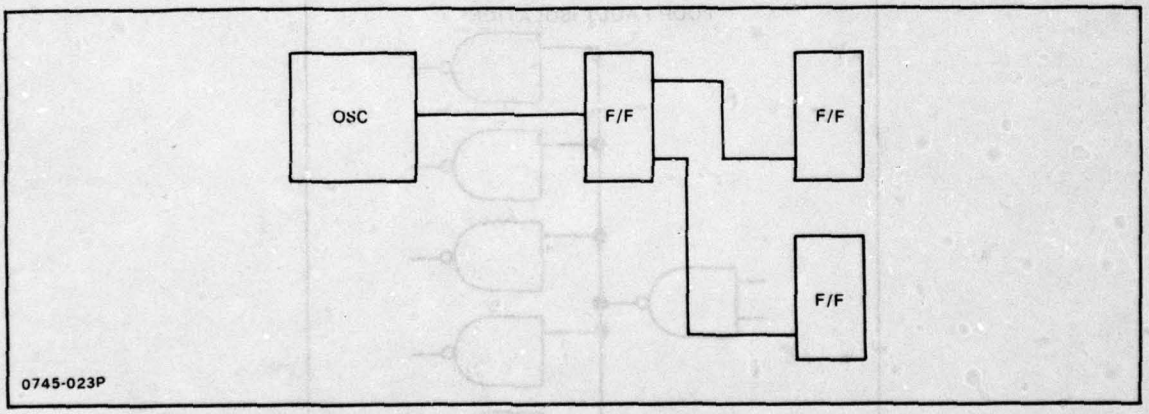


Figure 4-16 Unacceptable Design

There are several good testability corrections which can overcome this difficulty. One approach is to bring the oscillator output directly to a primary output pin. This will permit a direct check of whether the oscillator is functioning. Another approach is to add gates between the clock and its destination. This will allow the ATE to disable the clock and supply its own test clock (see Figure 4-17). An alternative would be to use a socket for the oscillator so it can be removed during test, and an alternate signal supplied from the ATE (see Figure 4-18).

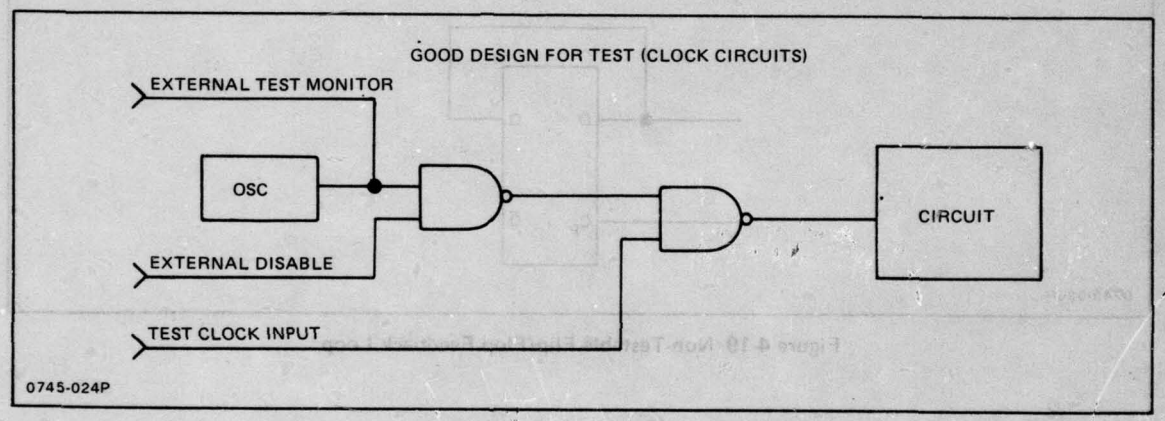


Figure 4-17 Design for Testability Oscillator Circuit

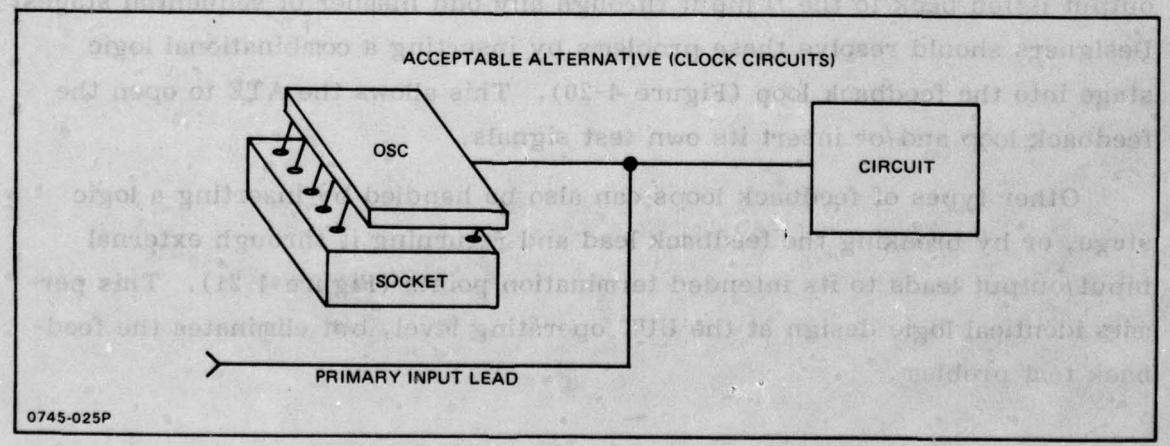


Figure 4-18 Use of Socket Aids Oscillator Testability

When using poly-phase clocks the same basic principles apply. Each clock phase should be monitored. Each phase should permit disabling by use of a test signal input, and each phase should have a clock override which permits substitution of an external clock from the ATE.

4.1.1.5 Handling of Feedback Loops - Feedback loops can make testing almost impossible. Certain circuit configurations using feedback should be avoided. Figure 4-19 shows a sequential stage with the "Q" output tied back to the "D" input.

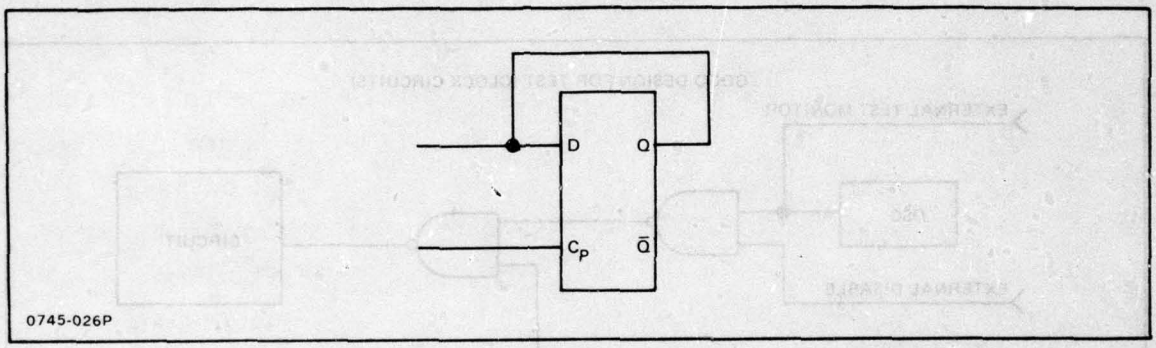


Figure 4-19 Non-Testable Flip/Flop Feedback Loop

Once the state of Q is superimposed on D, the stage is locked up and can't be used to check signal propagation. This same basic effect can occur if the Q output is fed back to the D input through any odd number of sequential stages. Designers should resolve these problems by inserting a combinational logic stage into the feedback loop (Figure 4-20). This allows the ATE to open the feedback loop and/or insert its own test signals.

Other types of feedback loops can also be handled by inserting a logic stage, or by breaking the feedback lead and returning it through external input/output leads to its intended termination points (Figure 4-21). This permits identical logic design at the UUT operating level, but eliminates the feedback test problem.

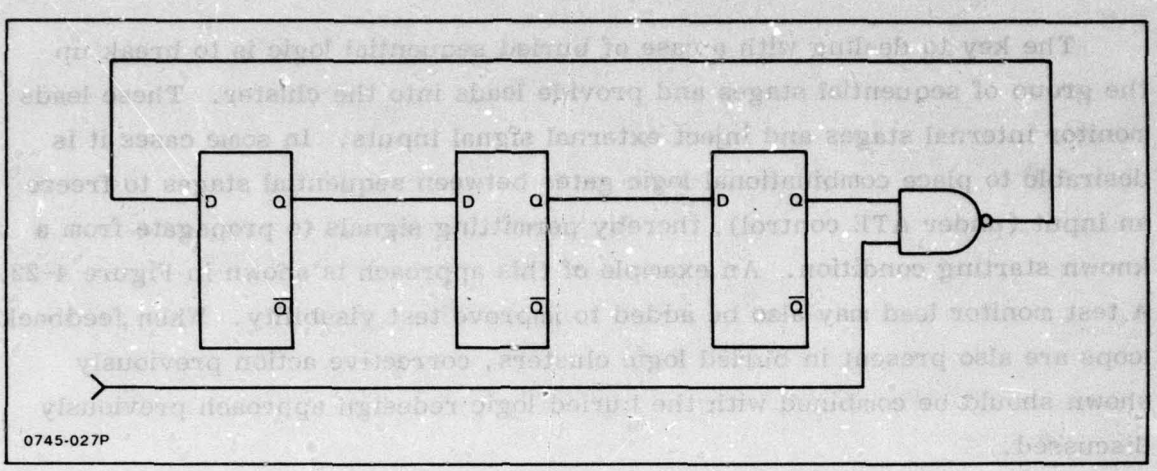


Figure 4-20 Externally Controlled Gate Breaks Feedback Loop

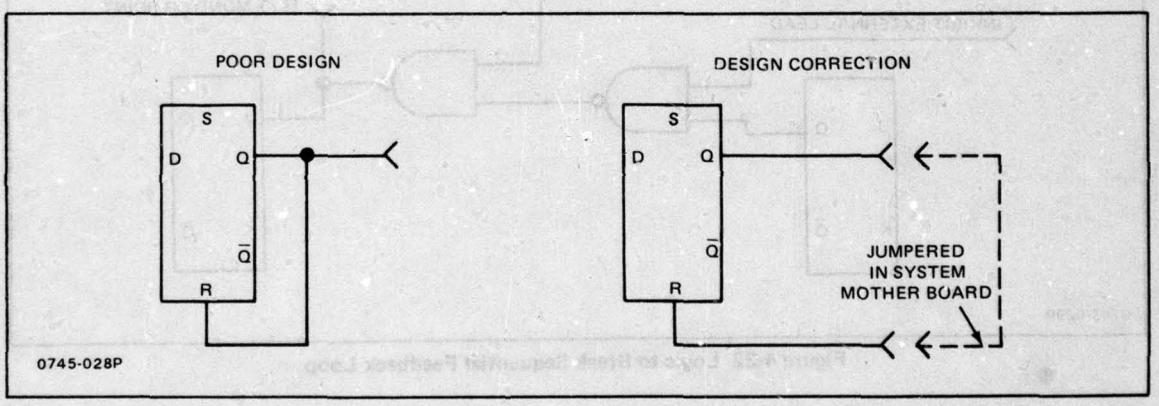


Figure 4-21 Feedback Loop Broken for PCB Test – Connected in System Interconnect Harness

4.1.1.6 Resolving "Buried Logic" Clusters and "Bottlenecks" - The logic circuits of a PCB become "buried" when several sequential stages are interconnected with no access to primary inputs or outputs. When the outputs of many logic stages (either sequential or combinational type) all reduce to pass through a single circuit internal lead, that lead or gate represents a "bottleneck" to proper test and fault simulation. Once either of these two conditions are present in a PCB, steps must be taken to improve testability.

The key to dealing with a case of buried sequential logic is to break up the group of sequential stages and provide leads into the cluster. These leads monitor internal stages and inject external signal inputs. In some cases it is desirable to place combinational logic gates between sequential stages to freeze an input (under ATE control), thereby permitting signals to propagate from a known starting condition. An example of this approach is shown in Figure 4-22. A test monitor lead may also be added to improve test visability. When feedback loops are also present in buried logic clusters, corrective action previously shown should be combined with the buried logic redesign approach previously discussed.

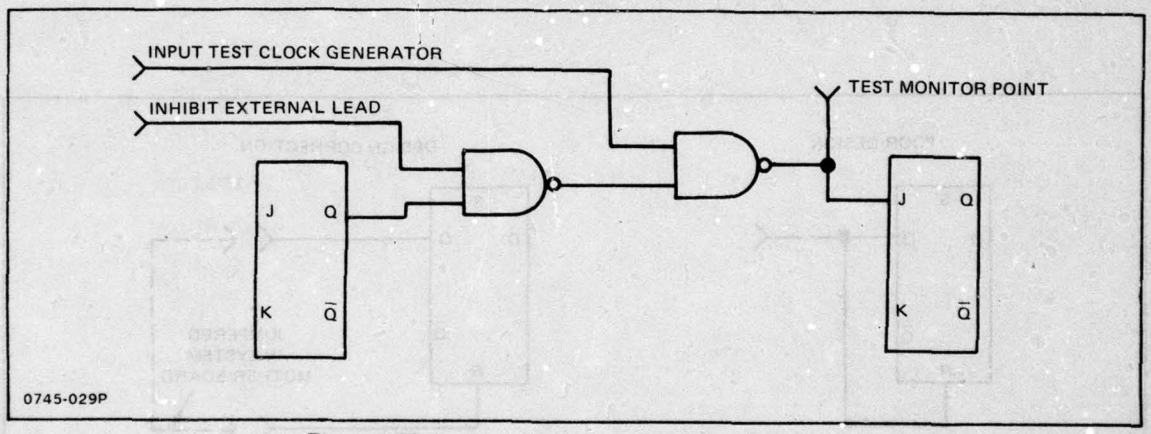


Figure 4-22 Logic to Break Sequential Feedback Loop

Logic bottlenecks such as shown in Figure 4-23 require good monitoring. Test points should be added on either the inputs or the outputs of the bottleneck, or in severe cases, an extra gate generator with external control lead should be used.

4.1.1.7 Testing Counters - When there is a buried counter, and no way to inject a clock pulse from the inputs (Figure 4-24), provision should be made for a test clock generator, either by modifying the clock circuit (Figure 4-17) or by converting the first stage of the counter to a test clock (Figure 4-7). It is good testability practice to provide a counter monitor point every three to four stages of the counter.

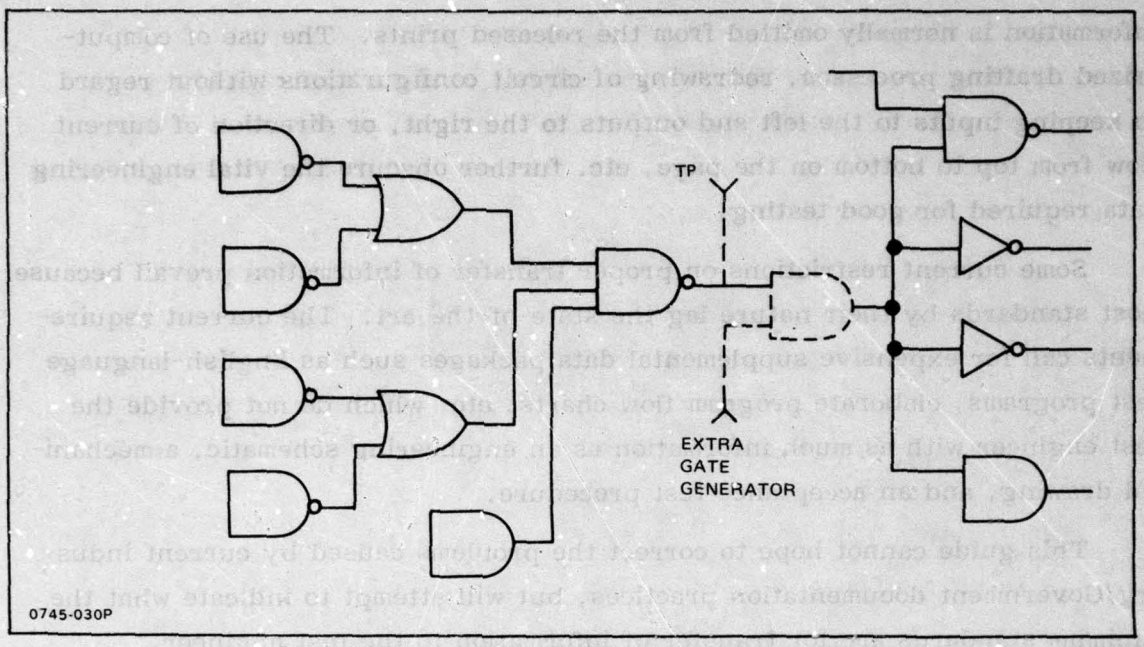


Figure 4-23 Gate Added to Control Circuit "Bottleneck"

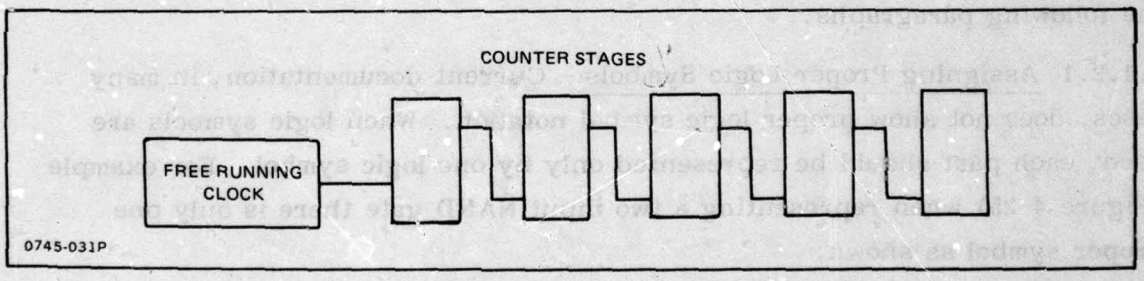


Figure 4-24 Buried Logic (Counters)

Counters which can be loaded and read by parallel signal lines are easier to exercise than those which must be accessed serially. It is recommended that all counters in the circuit have parallel access.

4.1.2 Testability Documentation Requirements

When the designer prepares documentation which will be used in test development work, the quality of this documentation becomes a significant testability consideration. Part of the difficulty commonly experienced by the test design engineer is that he is supplied with production drawings instead of the actual engineering drawings used to initially develop the design. Much information is lost in formatting to MIL-STD procedures. Important descriptive

information is normally omitted from the released prints. The use of computerized drafting processes, redrawing of circuit configurations without regard to keeping inputs to the left and outputs to the right, or direction of current flow from top to bottom on the page, etc. further obscure the vital engineering data required for good testing.

Some current restrictions on proper transfer of information prevail because most standards by their nature lag the state-of-the-art. The current requirements call for expensive supplemental data packages such as English-language test programs, elaborate program flow charts, etc. which do not provide the test engineer with as much information as an engineering schematic, a mechanical drawing, and an acceptance test procedure.

This guide cannot hope to correct the problems caused by current industry/Government documentation practices, but will attempt to indicate what the minimum standards are for transfer of information to the test engineer.

Criteria have been established for the documentation factors appearing in the following paragraphs.

4.1.2.1 Assigning Proper Logic Symbols - Current documentation, in many cases, does not show proper logic symbol notation. When logic symbols are used, each part should be represented only by one logic symbol. For example (Figure 4-25) when representing a two input NAND gate there is only one proper symbol as shown.

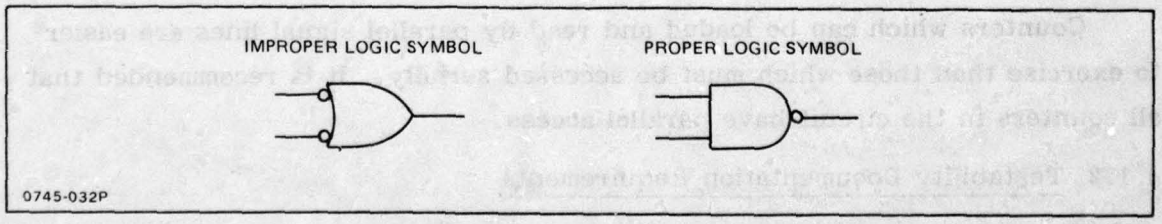


Figure 4-25 Use of Proper Logic Symbols

When this approach is not followed and software-oriented people control a design, it forces the test engineer to reverify circuit parts to see if parts drawn differently are really identical. This is time-consuming and unnecessary. By always using the same symbol for a logic function it is possible to avoid confusion and shorten the amount of time to debug a test program.

A second aspect of the "Proper Symbol" problem is the need to represent and correctly orient the leads into and out of a logic stage. If correct logic symbols are drawn inside the package outline (as per Figure 4-26), and pin designations are shown with proper logical names for each lead, there is nothing left to question. When the Figure 4-26(b) approach is used, device type number and equivalent internal circuit logic should be identified at least once on the schematic. The Figure 4-26(a) approach is preferred. One type of notation which is totally unacceptable is illustrated by Figure 4-27 which shows the same IC in a way totally misleading to the test engineer and devoid of any logic information.

The referenced ABC 1234-1 is not a standard industry commercial part and the pin designation shown, look like Pin 4 is an output when it is actually a gate input of U7B (see Figure 4-26(a)). No function designations such as

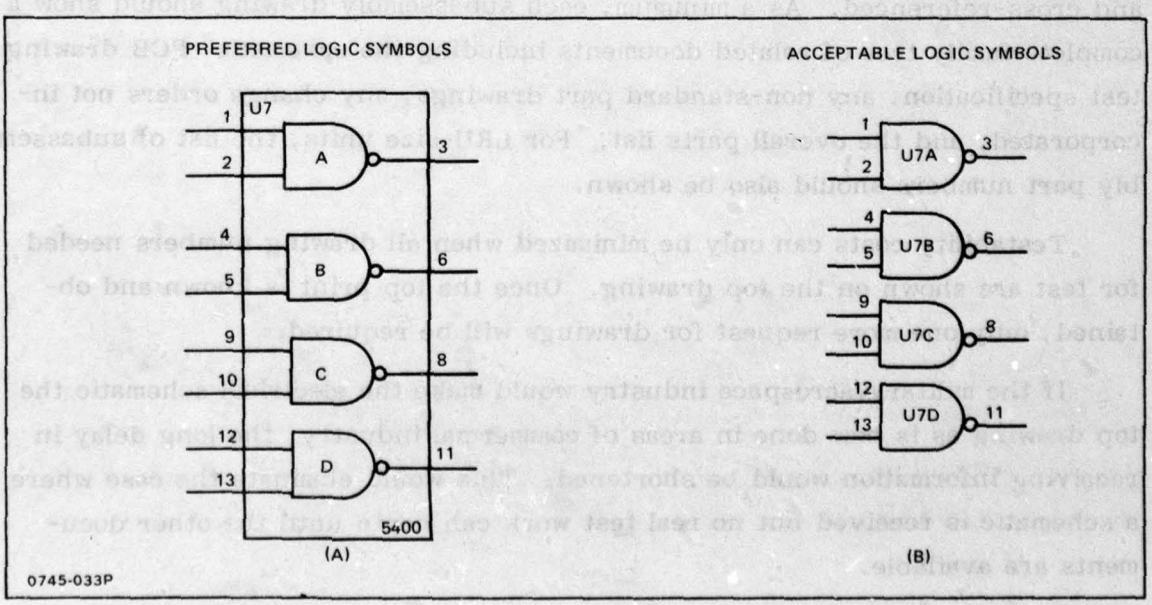


Figure 4-26 Preferred or Acceptable Logic Symbols

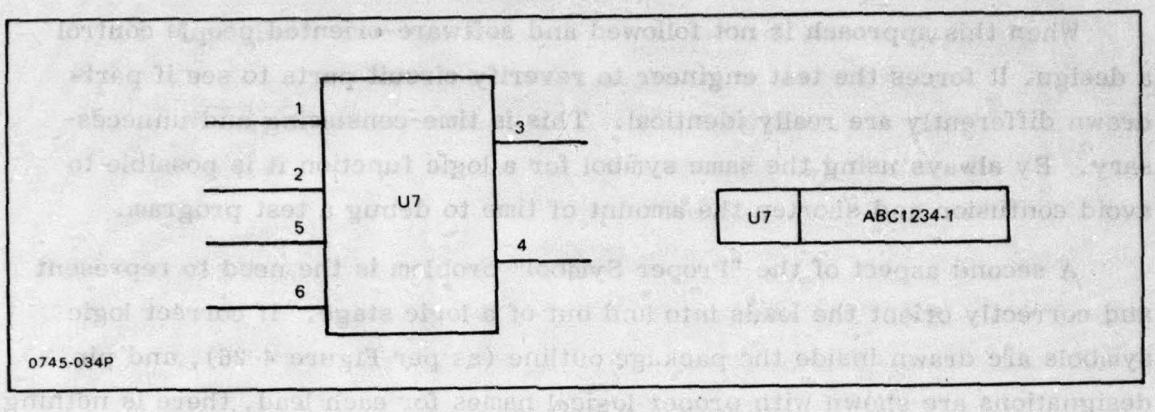


Figure 4-27 Unacceptable Logic Symbols

"Input 1 Gate A," "Input 2 Gate A," etc. are given. In certain cases, the assumed throughput of a function will lead to the wrong output pin. When no other information is available, this type error can make an entire test circuit model worthless. Proper use of logic symbols is most important for good testability.

4.1.2.2 Cross Referencing of Drawings - Efficient and effective design of a test program set depends on how well the various applicable documents are indexed and cross-referenced. As a minimum, each subassembly drawing should show a complete family tree of related documents including the schematic, PCB drawing, test specification, any non-standard part drawings, any change orders not incorporated, and the overall parts list. For LRU-size units, the list of subassembly part numbers should also be shown.

Testability costs can only be minimized when all drawing numbers needed for test are shown on the top drawing. Once the top print is known and obtained, only one more request for drawings will be required.

If the military/aerospace industry would make the electrical schematic the top drawing as is now done in areas of commercial industry, the long delay in receiving information would be shortened. This would eliminate the case where a schematic is received but no real test work can begin until the other documents are available.

4.1.2.3 Non-Standard Parts - Many companies use non-standard parts as a means to prevent competition from being able to do legitimate test work. When documentation is forwarded without non-standard parts data, test work is impeded. In the preferred approach, the internal logic diagrams with package pin designations and proper logic symbols are shown either as part of the circuit schematic or shown once at the edge of the schematic as a referenced figure.

4.1.2.4 I/O Pin Designations - Inputs and outputs should be brought to the edges of the schematic so that requirements for test interfaces can be quickly established. It is preferable to bring inputs out to the left and outputs to the right. In any case, inputs should be clearly distinguished from outputs by a method similar to Figure 4-28, with directional arrows on the leads.

No input or output should be contained in the inner portions of the detailed schematic. Each lead should be labeled with a unique name to facilitate identification of connections between assemblies.

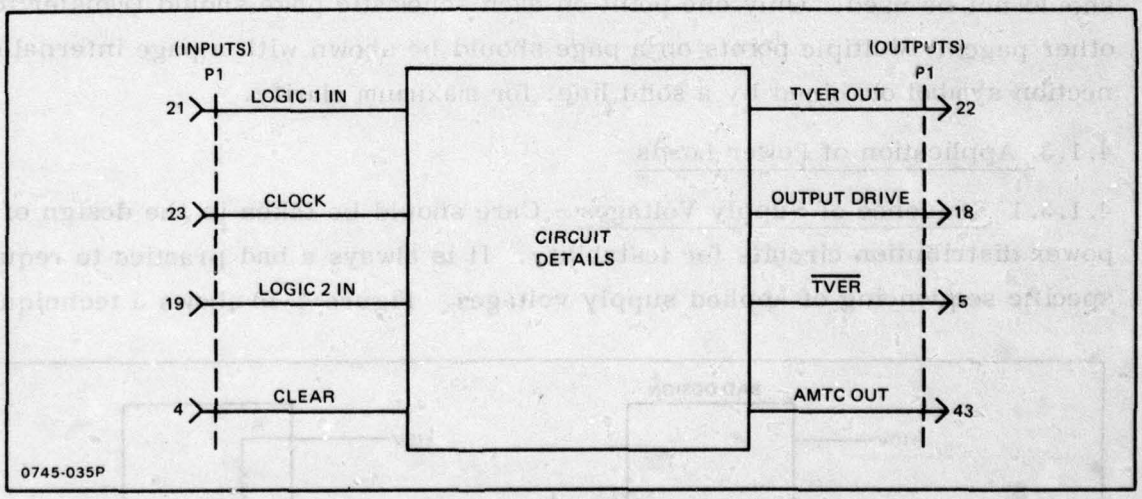


Figure 4-28 Arrows Distinguish Inputs from Outputs

4.1.2.5 Proper Page Connectives - Without properly written page connectives, for multipage complex schematics, it becomes an almost impossible job for the test engineer to tabulate interconnecting signal paths. This condition will lead to days of extra and unnecessary engineering effort.

The circuit designer should properly annotate all such leads to show to-from information. Sector of page and page number should be given for each interconnection (see Figure 4-29). In addition, the point 4 shown on page 3 of the figure

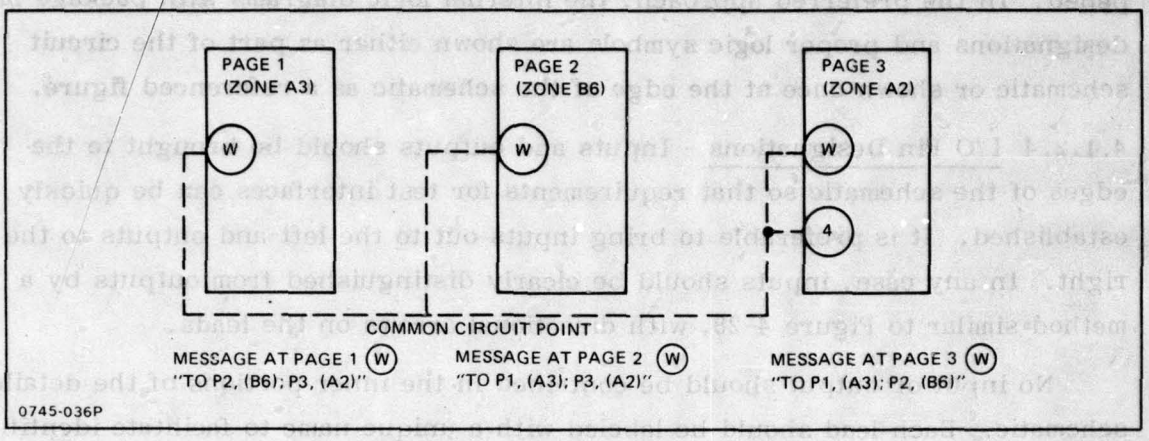


Figure 4-29 Use of Proper Page Connectives

should not be used. Only one point on each schematic page should transfer to other pages. Multiple points on a page should be shown with a page internal connection symbol or joined by a solid line, for maximum clarity.

4.1.3 Application of Power Loads

4.1.3.1 Sequence of Supply Voltages - Care should be taken in the design of power distribution circuits for testability. It is always a bad practice to require specific sequencing of applied supply voltages. Figure 4-30 shows a technique

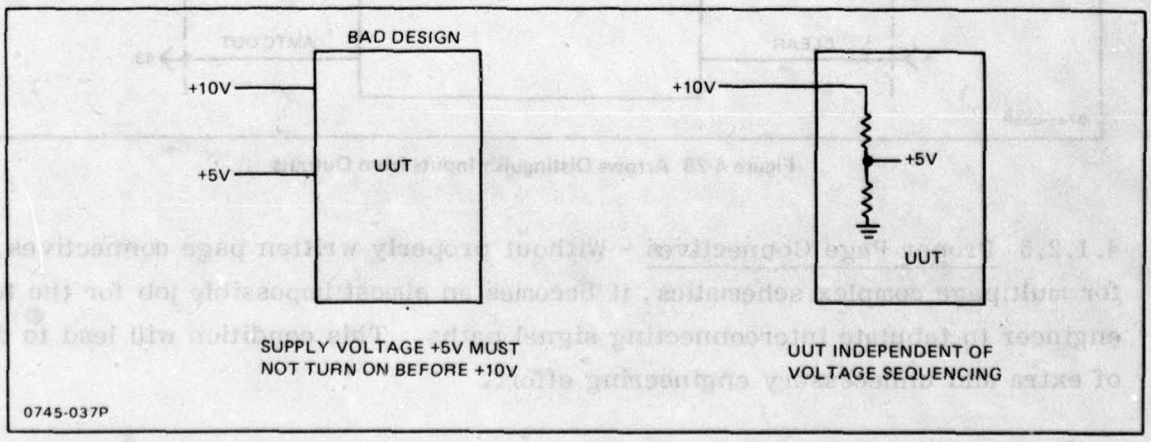


Figure 4-30 Circuit Divider Insures Voltage Sequencing of Required Supply Voltages

to eliminate sequencing of supply voltages. This approach can be extended to use shunt or series regulators internal to the UUT.

When an excessive number of supply voltages is required to test a circuit a similar redesign could be used to reduce their number.

For circuits such as lamp drivers which require relatively high current output stages, good design for testability is to use low power pull up collector load resistors on the output stages as part of the circuit. This permits correct logic operation (Figure 4-31) without the use of external loads. When the use of extra loads for multiple outputs is required, their size can be reduced by use of diodes with a common resistor (Figure 4-32). Power ratings of the reduced design must be calculated to stay within component power limits for short circuit cases.

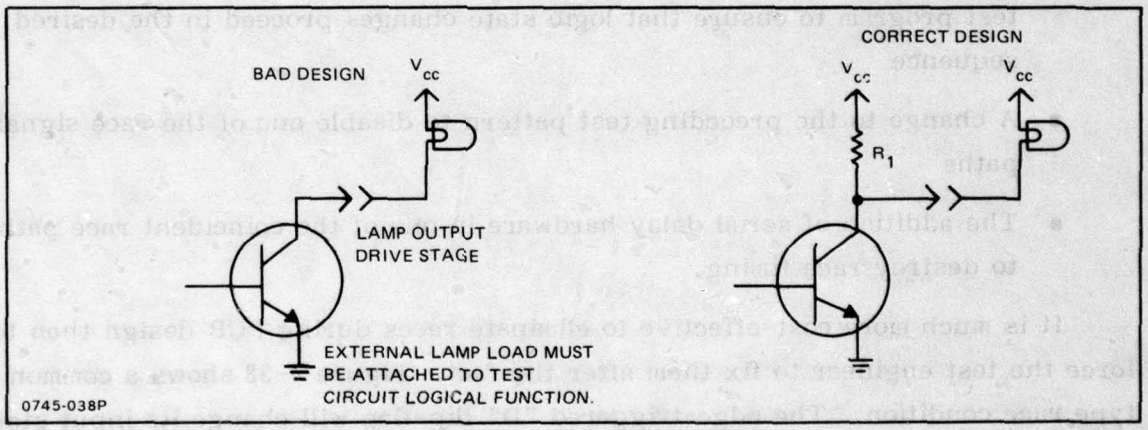


Figure 4-31 Output Switch Uses Pullup Resistor

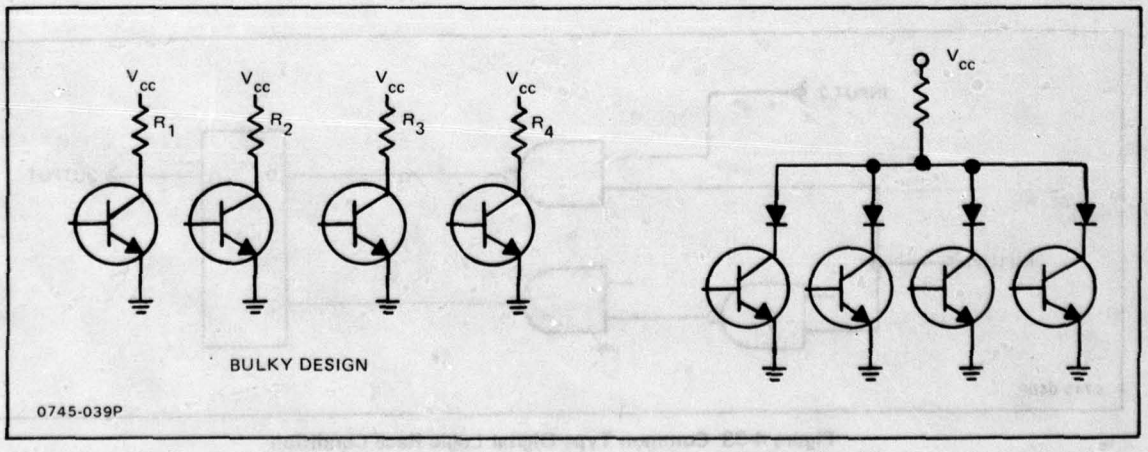


Figure 4-32 Use of Diodes Can Reduce Size of ID Test Loads

4.1.3.2 Uniform Power Pins - When more than one subassembly is associated with the circuit to be tested, power voltages and returns should be wired to the same corresponding pin of each subassembly. This reduces the complexity of ATE interface devices.

4.1.4 Miscellaneous

4.1.4.1 Clock Race Problems - Latent clock race problems can easily present themselves when digital test patterns are generated by automated computer processing. The circuit design should be reviewed to locate latent race conditions and design corrections should be made. Three types of design changes are currently used to correct races during test:

- The use of additional test patterns inserted at the race point of the test program to ensure that logic state changes proceed in the desired sequence
- A change to the preceding test pattern to disable one of the race signal paths
- The addition of serial delay hardware in one of the coincident race paths to destroy race timing.

It is much more cost-effective to eliminate races during PCB design than to force the test engineer to fix them after the fact. Figure 4-33 shows a common type race condition. The edge-triggered "D" flip-flop will change its input state before the clock pulse edge reaches the flip/flop. This causes an improper output

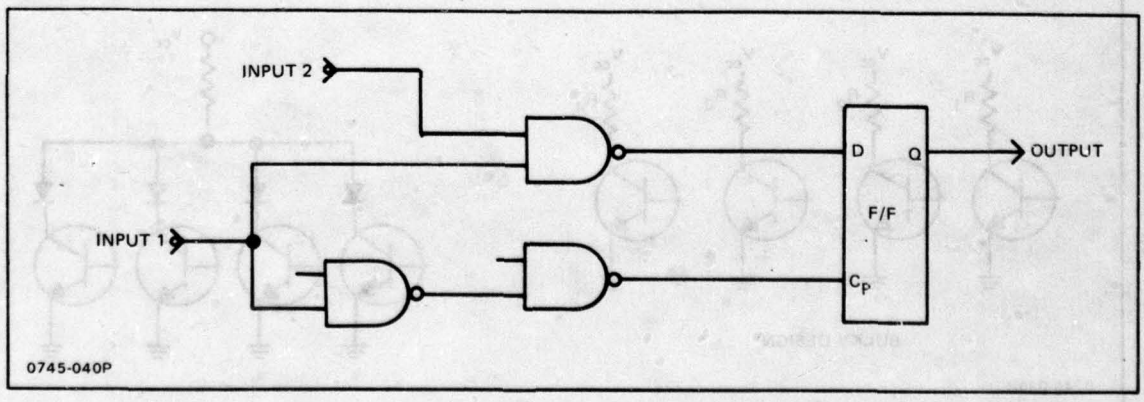


Figure 4-33 Common Type Digital Logic Race Condition

when the flip/flop is triggered. The race problem can be overcome by holding Input 2 low until the next test pattern which will maintain a logic "1" on the D input.

While a buffered test pattern using input 2 will solve the race problem for one test pattern, a basic hardware solution would solve the problem every time. Figure 4-34 shows two such solutions.

In the first of these two approaches, the circuit is modified to split input 1 into two inputs. The circuit will function identically in the system since the separated inputs are rejoined in the interconnection harness. During testing the automatic pattern generator controls each of the two leads independently and is unaware that they are related. A complete test can now be made without a race.

In the second case (Figure 4-34), input 1 can remain the same but two extra invertors are serially added in the D input path. Thus, the data will always change after the desired input is clocked to the output.

Basic circuit designs should eliminate situations where the clock and data input for one sequential circuit is derived from a common input, or where two clock lines from a common source go through different delays to trigger interrelated sequential circuits.

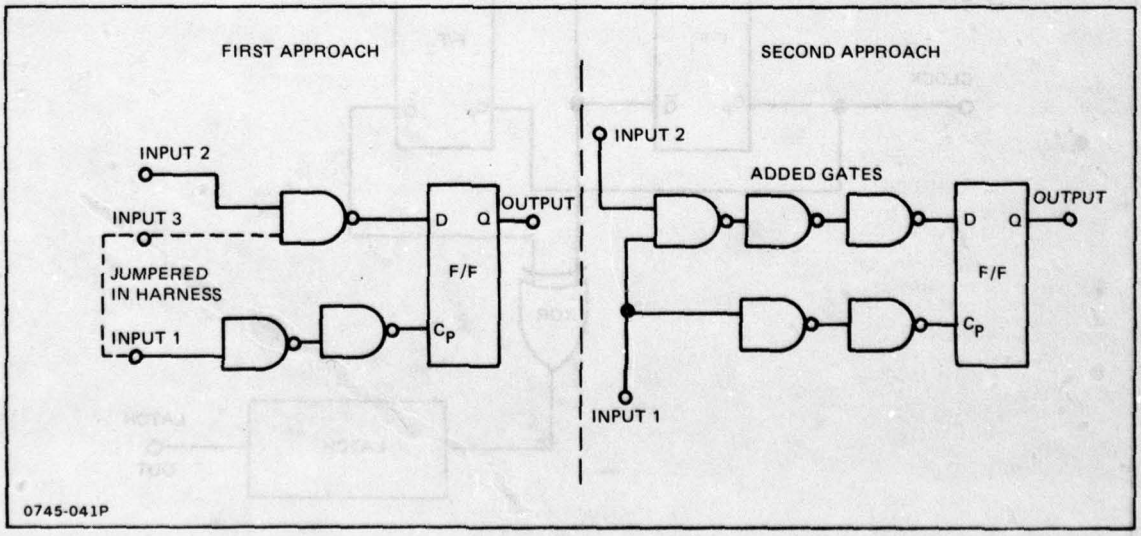


Figure 4-34 Techniques to Eliminate Digital Race Problems

Another possible race condition can occur in the network of Figure 4-35. The exclusive OR gate will remain at a "0" output for either two "0" inputs or two "1" inputs. As F/F1 triggers F/F2 there is a possibility of unlike inputs to the exclusive OR gate during the transient instant ("0" to "1" or "1" to "0") even though like inputs are present before and after the clock. There is some possibility that the transient trigger pulse will activate the latch to a false state. This is another form of a race condition.

There are many similar types of digital races which can occur in complex circuits. Ability to change the hardware prior to a commitment to production is of paramount importance in solving race problems. This takes a large burden away from the test development engineer who otherwise is limited to work-arounds and to solving race conditions by extensive software manipulation.

4.1.4.2 Monostable Multivibrators - Buried monostable circuits present a formidable problem when using Automatic Test Generation. Good testability practice can reduce the test difficulty by bringing the input trigger lead and the output lead to external pins. In addition, a dual gate structure should be used (similar to Figure 4-17) when the monstable circuit drives other sections of the PCB.

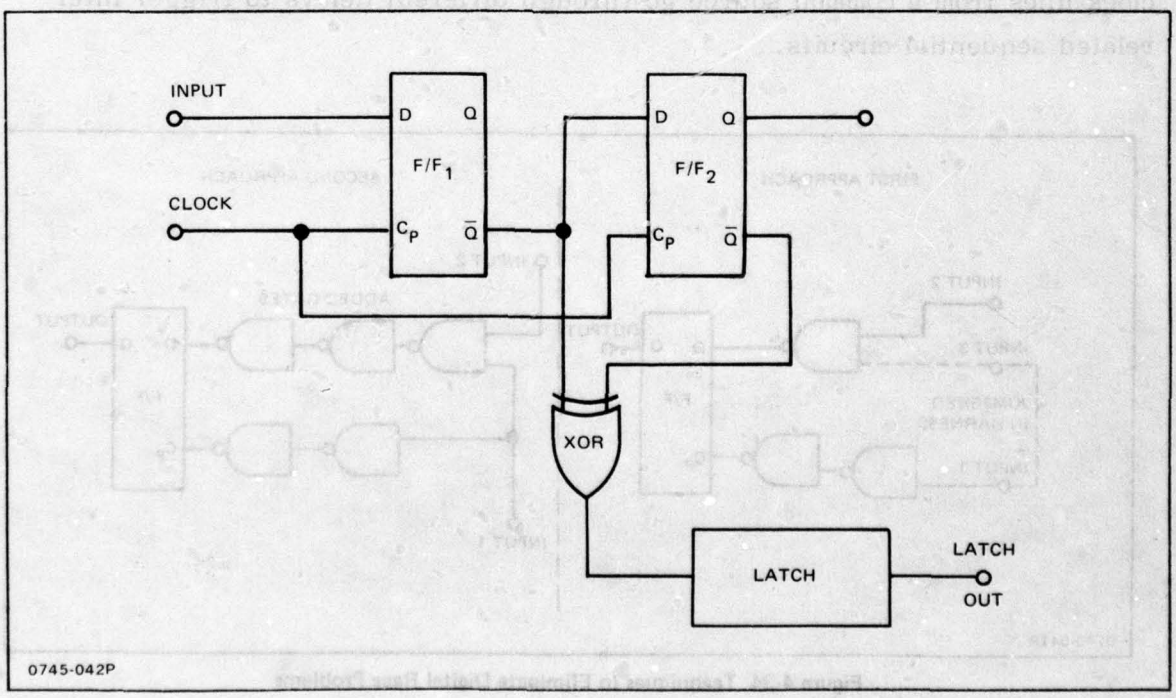


Figure 4-35 Race Condition Through Exclusive or Gate Can False Trigger Latch Circuit

The extra gates permit the monostable output to be inhibited and allow insertion of an external test signal to drive the circuitry in place of the monostable.

If these testability modifications are not used, the testing of built-in monostables becomes a nearly impossible task requiring extensive manual testing to achieve any degree of fault detection.

4.1.4.3 High Frequencies - Use of high frequency signals on a PCB complicates testing. High frequency signals in excess of 10 MHz must be supplied on direct coaxial lines with proper termination.

When system requirements make use of high frequency signals unavoidable the testability engineer may be limited in what can be done to ease the test problem.

In some cases he can design around high frequency signals. When serial data must be loaded at a 10 MHz rate, the circuit can be redesigned to permit acquisition of data by parallel input lines. None of these solutions are very satisfying and normally the test engineer must live with the high frequency problem.

4.1.4.4 Use of Potentiometers - Adjustments performed during a test program make the testing much more complex. The objective of a design for testability must be to eliminate potentiometers wherever possible.

If the purpose of an adjustment is to set a precise voltage which is not subsequently readjusted, it is preferable to use a 3-resistor voltage divider (see Figure 4-36), where R_S is a selected precision resistor custom-tailored to each circuit.

4.1.4.5 Test Point Isolation - Test points should be properly terminated by a resistor when space on the PCB permits. This prevents (Figure 4-37) possible shorting during probing.

4.1.4.6 Orientation of IC Packages on PCB - For ease of testing it is preferable to align the IC packages on a PCB in one direction (Figure 4-38). Also, each IC package when aligned should have identical orientation of power pins to minimize probing of incorrect circuit points.

IC packages should be numbered in a logical order by rows and the designations clearly labeled on each side of the PCB.

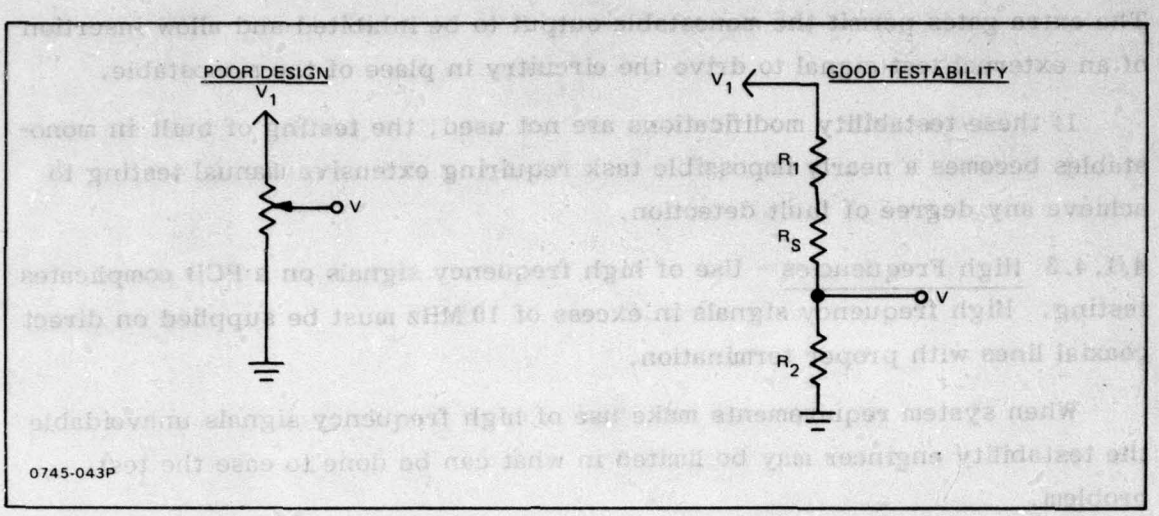


Figure 4-36 Divider Network Eliminates Adjustment

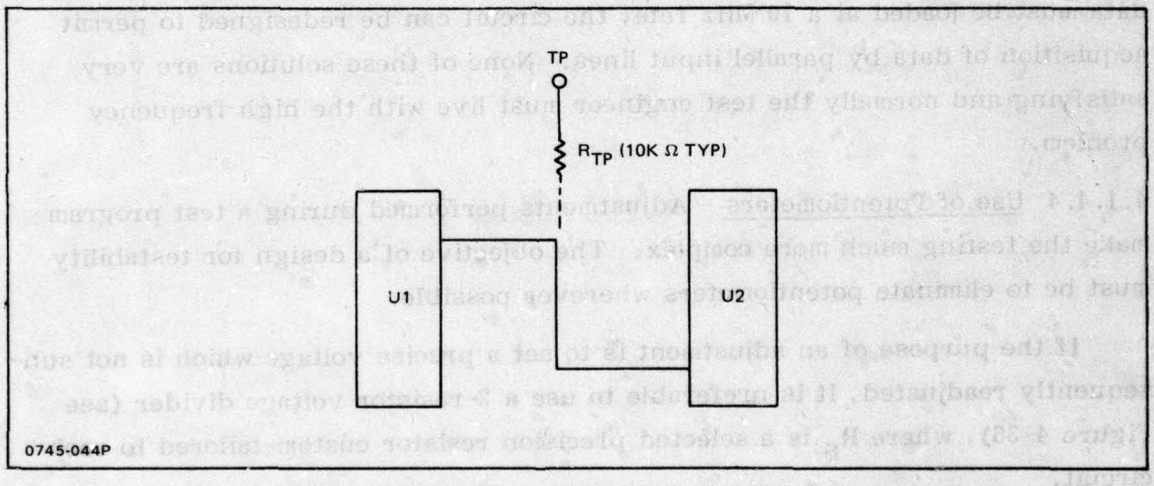


Figure 4-37 Resistors Provide Isolation for Probe Test Points

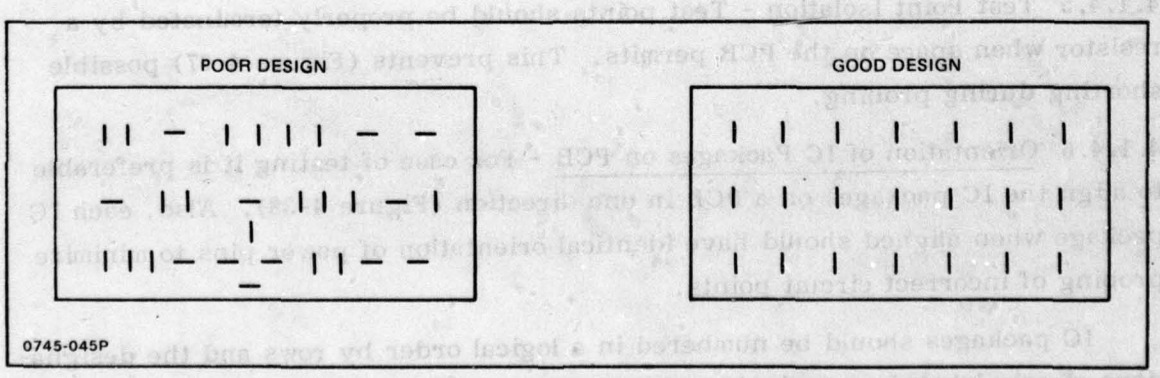


Figure 4-38 Orientation of IC Packages on PCB

4.1.4.7 Testing of Microprocessors, Memories and Other Complex Parts - Several design guidelines apply to the use of microprocessors, memories and complex parts. When the internal logic configuration of a complex part is unknown, the part cannot be modeled for automatic test generation and the test work must take place around the part. Use of a socket for this type of part becomes almost mandatory (Figure 4-39). The test procedure is to remove the part from the circuit and test the remaining circuit parts with it removed using (if necessary) a plug-in head as a test connector in the socket. After any faults are repaired and a

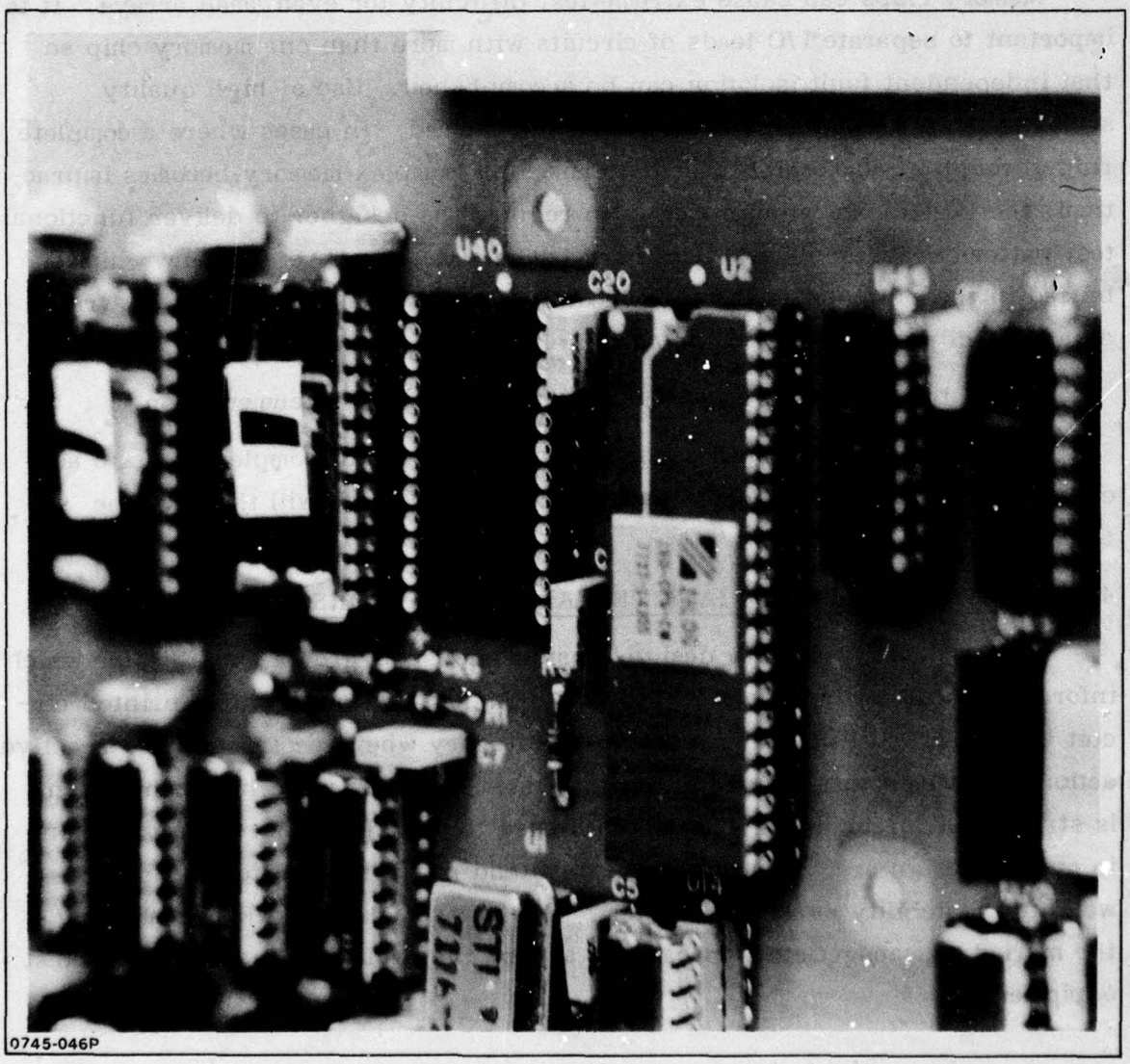


Figure 4-39 Testability of Microprocessor PCB Circuit Improved by Use of Socket

good end to end test passes, remove the test socket connector and plug the complex part back in. Then perform a functional test on the overall circuit. If the functional test fails, replace the microprocessor. In general, it is good design practice to bring out all the pins of a microprocessor or memory chip to external I/O connectors. For cases where a microprocessor has tri-state logic outputs, test patterns can switch all these points to the open or quiescent logic state. The non-microprocessor tests can then be performed without forcing a part removal and this procedure can be followed with overall functional tests.

Memory chips can cause extreme test difficulty for even small arrays. It is important to separate I/O leads of circuits with more than one memory chip so that independent fault isolation can be accomplished. Use of high quality sockets for all memory arrays is strongly preferred. In cases where a complete ring-through of all possible test patterns for a complex memory becomes impractical, the best technical approach is to require the designer to deliver functional test patterns representative of memory usage. Cases where a memory chip is buried in the middle of PCB logic without direct test access to its read, write data and address lines are to be absolutely avoided.

The data contents of all ROMs must be provided as documentation.

When IC users ultimately force the manufacturers of complex parts to accurately disclose internal logic configuration, these parts will then become testable.

4.2 SYSTEM/MANAGEMENT/ATE TESTABILITY FACTORS

System-level testability design considerations for groups of PCBs for which information will not be found in the documentation for an individual printed circuit board, must be placed in a different category when recommending corrective action. These factors depend on how a system is configured, how management is structured, or upon the specific ATE used to test the PCBs. The variations in system design are so numerous that it would be impractical to attempt a weighted testability evaluation system. The same holds true when evaluating the myriad of management approaches, and/or the proliferation of different test equipment.

The above cannot be ignored, however, since the cost of PCB testing can be greatly reduced by good testability design practices and management. One major way to simplify the testing problem at the system-level is to make all system power, grounding, board connectors, etc. common and identical so that a maximum number of PCBs can be tested on a common ID. The fewer IDs required for an overall system, the lower the cost to test. Maximum use of circuits which can be tested by automatic test generators is recommended.

The best approach to presenting system factors is to show them as a check list with an explanation of each factor relative to its impact on testing. These factors are grouped into four general categories:

- System Interface
- Management
- System Hardware
- System Power.

4.2.1 System Interface Factors Checklist

Limit the Number of Different Part Types Used - An extremely significant factor which can greatly aid in reducing spare parts inventory as well as handbooks and prints.

Limit Types of Logic Families - This system factor reduces test complexity by reducing the number of logic voltage levels.

Fail Safe Design - UUT I/O Lines - Careful attention to this detail reduces chances for damage while testing.

System Clock - External Disable - This design feature permits the tester to control internal timing operations from outside the unit under test.

Functional Packaging - This factor is difficult to define with any precise criteria. Clever design can, however, produce a system which virtually eliminates all but functional I/O leads between LRU modules. This makes isolation of a fault to the module level easy and keeps use of auxiliary test equipment to a minimum.

Proper BIT Application - Well-designed BIT lowers the cost of testing by limiting test work to modules which actually are defective. It also assists in fault isolation.

Feedback Loops Open for Test - Good system design will build in leads to a test connector which will permit breaking loops for test purposes. This greatly simplifies locating of a faulty internal subassembly when several are involved in a feedback loop.

Well Chosen Test Detect/Isolate Levels - Good system design makes provision for fault detection and fault isolation to the lowest possible level economically approachable.

No Reconvergent Fanout Between LRUs - For digital units, care must be taken not to form parallel paths of logic from a single source point which converge at a second single point.

Design For ATG Compatibility - Sections of independently testable digital logic should be limited to a complexity compatible with the capabilities of the intended automatic test generation system.

4.2.2 Management Factors Checklist

System Configuration Control - A first prerequisite for good management of test program development is to establish a simple and clearly understandable method for defining system configuration. The documentation must show each LRU; interrelate each removable unit (RU) with all possible configurations of the LRU; relate circuit board, assembly, and schematic to an RU for each configuration; tie in test program and ID nomenclatures for each version of each LRU; and document all support-of-support testable assemblies for each configuration.

A second part of good system configuration control is to maintain accurate records of test equipment and spares at all field sites, so when a problem occurs in a remote location, corrective action can be taken immediately.

Use a Test System with Real Time Compiler - Many test development projects use test systems which do not have a capability to change a test program while on the test station. Use of an offline compiler which is not part of the on-station

operation places an added burden on the test engineer which could more than double test program development time. Good management will mandate real time inline compilation with file security provisions which limit this capability to authorized personnel.

Use of Proper Test Diagrams - The overall cost to test can be reduced by putting as much of the hardware test diagrams as possible on one print. When necessary, more than one sheet can be used, in which case a functional sector division of the test diagrams should be defined which can "stand alone" without large dependence between sheets.

For selected key tests, the test diagram can be modified by accenting leads to stand out while retaining the rest of the test information in the background.

Use of this approach reduces the difficulty of identifying "sneak" paths or of finding sources of cross coupling signals in the overall test wiring. Such problems can cause delay and tie up test stations. Good test diagrams reduce the risk of such problems by providing test visibility.

Proper System Labeling - Good management will give careful attention to the formulation of a simple, clear system of labels. Proper part marking on the PCB helps to quickly identify components. Marking polarity of capacitors, terminals of batteries, diode directions, etc. helps ensure proper manufacture of the assembly. The use of matching arrows to show proper direction of PCB insertion is recommended.

Wherever possible, the PCB should be marked with actual pin numbers, and not force the user to employ a mental translation process because of the designers attempts to make a socket general.

4.2.3 System Hardware Checklist

Use a Common PCB Connector - Good testability practice is to use the same basic connector for as many PCBs as possible. If the connector is keyed, the keying should be "defeatable" to allow for ease of testing.

Use a Common ID for the Maximum Number of PCBs - The fewer the number of separate IDs required, the lower the overall test cost. Care should be taken to group similar PCBs with a common ID.

4.2.4 System Power Checklist

Power Supply Sequencing - The need to sequence the application of power supplies is very undesirable. The system design should require circuitry such that any sequence of applied voltages is acceptable.

Common Pins for Power/Ground Leads - Good system design simplifies test work by keeping power and ground pin assignment consistent for each module or PCB in the system. Pins should be selected such that power and ground do not occur on adjacent pins.

Standard Grounding Philosophy - Use of a common or standard grounding technique for all modules and circuit designs further simplifies the testing problem.

4.3 PCB TESTABILITY EVALUATION SYSTEM

The Testability Evaluation System rates PCBs in terms of four basic test factors and 30 negative testability factors. Basic test factors define a score on a positive scale of 0 to 100%. This represents how closely the generic design of the PCB approaches optimum testability. The negative testability factors are penalties for bad design practices. The total negative score is subtracted from the total positive score to produce a net total score. The net total score is the measure of PCB testability.

Negative factors can usually be reduced by the designer using the testability design methods recommended in this guide. The process used to identify and correct testability problems is based on objective mathematical standards. The rating process is designed to require less than eight working hours per PCB evaluated. The evaluation system takes into account known factors relating to the cost of testing. Automatic testing considerations and proper documentation are also key inputs to the evaluation process.

Examples of remedial testability design methods are divided into five main areas; circuit structure (with sequential circuit and ATG factors), special parts (microprocessors, memories, VLSI, etc.), documentation, power application, and miscellaneous (tolerance, adjustments, high frequency, fail safe, mechanical, etc.). In each area, specific design corrections are recommended to reduce the difficulty of testing.

4.3.1 Use of the PCB Testability Evaluation System

When initiating a testability evaluation, the following is mandatory:

- Schematic/logic diagram
- Parts list
- Specifications and internal logic of all PCB parts
- All documents must be legible
- Configuration of the PCB and its documents must be clearly stated and identical.

Do not proceed with the evaluation unless all of the above items are present and accounted for.

The following provides a step-by-step procedure to conduct a PCB testability evaluation. The evaluator will require the following:

- A Node Accessibility Score Sheet (Figure 4-40)
- The PCB Testability Evaluation Score Sheet (Figure 4-41)
- The PCB Testability Evaluation System (Subsection 4.4).

The procedure will refer to the above as needed in the evaluation.

COMPILATION OF BASIC (POSITIVE) FACTORS

STEP 1

Use the Node Accessibility Score Sheet (Figure 4-40) and the schematic/logic diagram, to trace each primary input lead to all its termination points in the circuit. Place a mark in the score sheet box for each case which corresponds to the number of components tied to that lead under the appropriate column in the top half (Access) part of the form. When five or more parts are connected to a single input, circle that input lead on the schematic with a red pencil. Put a pencil check on each termination point so the same path will not be retraced later. Group the marks made in the numbered boxes by multiples of five or ten to make counting up the total easy.

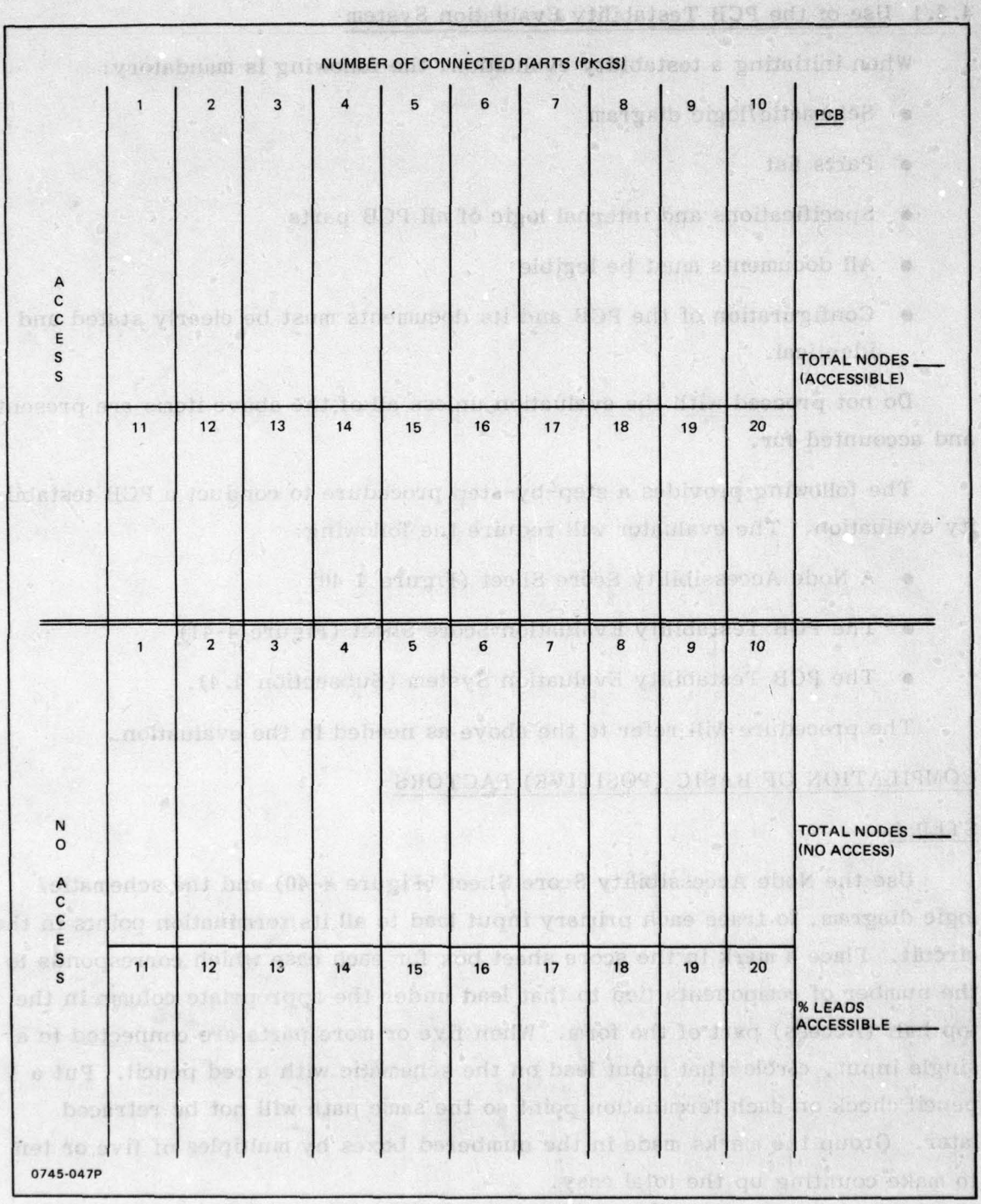


Figure 4-40 Node Accessibility Score Sheet

FACTOR	DESCRIPTION	SCORE	POSSIBLE RATING	ACTUAL RATING	COMMENTS
B1	Percent Nodes Accessible		30%		
B2	Proper Documentation		25%		
B3	% of Sequential Ckts		25%		
B4	PCB Complexity Count		20%		
	Total Basic Score		100%		
N1	Monostable Ckt		-%/Inst		
N2	Counters (Pkgs x Stgs)		-%/Inst		
N3	Max. No. Function Blocks/ Node (No Access)		-%/Inst		
N4	Max. No. Function Blocks/ Node (Accessible)		-%/Inst		
N5	Seq. Supply Voltages		-10%		
N6	Non-Remov. Memories		-%/Inst		
N7	Non-Rem. Buried Memory		-%/Inst		
N8	Removable Complex Part		-%/Inst		
N9	Non-Rem. U-Proc, VLSI		-10%/Inst		
N10	Init. of Seq. CKTS		-%/Inst		
N11	Ext. Loading Req'd		-5%		
N12	Different Logic Types		-%/Inst		
N13	Buried Seq. Logic		-%/Inst		
N14	I/O Pins Distinguished		-3%		
N15	Excess Warm-up Time		-3%		
N16	Tolerance		-%/Inst		
N17	High Power		-%/Inst		
N18	Critical Frequency		-5%		
N19	Clock Lines		-20%		
N20	Ext. Test Equipment		-%/Inst		
N21	Environmental		-10%		
N22	Adjustments		-%/Inst		
N23	Complex Signal Inputs		-%/Inst		
N24	Redundant Logic		-%/Inst		
N25	No. of Logic Voltages		-1%/L.V.		
N26	No. of Power Supplies		-1%/P.S.		
N27	Schematic Connectives		-20%		
N28	I/O Pin – Schematic		-5%		
N29	Dual Pin Designations		-3%/Inst		
N30	Symbols on Schematic		-5%		
	Total Negative Score				
	Net Total Score				

0745-048P

Figure 4-41 PCB Testability Evaluation Score Sheet

STEP 2

Repeat STEP 1 for each output lead.

STEP 3

Count the number of parts connected to each internal node (wiring junction point) and place a mark in the score sheet box which represents the number of parts connected to each node. (Since the internal nodes are inaccessible, these marks are made on the lower half of the form). When four or more parts are connected to the same node, circle the node at a convenient point with a red pencil. Place a pencil check on each termination point to prevent retracing the line later.

STEP 4

Total up the number of "Accessible" nodes and record their number in the Nodes Accessible blank of the Score Sheet.

STEP 5

Total up the number of "No Access" nodes excluding those which connect only one or two parts. Record this total in the Node Inaccessible blank on the Score Sheet.

STEP 6

Calculate the percent of nodes accessible:

$$\% \text{ nodes accessible} = \frac{\text{Total Count - Step 4}}{\text{Total Count - Step 5}} \times 100\%$$

Record this result on the Score Sheet. Also, enter this result on the PCB Testability Evaluation Score Sheet (Figure 4-41) as the score for the first rating factor. Convert this score to an actual rating by using the PCB testability evaluation system (Subsection 4.4) which converts the raw score to a weighted percentage. Enter the weighted percentage in the rating column of the PCB Testability Evaluation Score Sheet.

STEP 7

Proceed to Factor B2 of the PCB Testability Evaluation System (Subsection 4.4) and total up the percentage points for documentation items (a) through (f).

Points are awarded if requirements are met or exceeded. Enter total percentage in actual rating column of PCB Testability Evaluation Score Sheet.

STEP 8

Proceed to Factor B3 of the PCB Testability Evaluation System (Subsection 4.4). Using the PCB parts list, add up the total number of sequential IC packages. Divide the number of sequential packages by the total of all IC packages. (If discrete parts are used on the PCB, only count functional groups of discretes as equivalent to one IC). Score Sequential Groups and Combinational Groups in appropriate areas. Enter the percent of sequential circuits in the "Score" column of the Score Sheet and convert this value using Subsection 4.4 scale factors to get the actual percentage rating. Enter actual percentage on the Score Sheet.

STEP 9

Using the B4 instructions of Subsection 4.4, add up the total counts of all sequential circuit parts. Convert this total count to an actual rating percentage using the table in Subsection 4.4. Enter this actual percentage on the Score Sheet.

STEP 10

Add the actual ratings for Basic Factors B1 through B4 to arrive at the "Total Basic" score and enter this on the Score Sheet.

COMPILATION OF NEGATIVE FACTORS

STEP 11

Check PCB to see if there are any monostable circuits. Assess how these must be tested, and assign appropriate penalties as per the N1 section of the PCB Testability Evaluation System (Subsection 4.4).

STEP 12

Using the N2 factors of the PCB Testability Evaluation System, evaluate possible penalties and make the appropriate entries on the Score Sheet. Counters are considered accessible if a signal can be directly input. The count of stages starts from each direct input and continues until the final stage of the counter is reached, or until a point where another input can be injected is reached. If

there are test points within the counter, the penalty is reduced (see N2 (a) and (c) factors).

STEP 13

Using the filled out Node Accessibility Score Sheet, add up the total instances of inaccessible (bottom half of chart) nodes for groups of 4, 5, 6, ---N packages separately by group. Using the PCB Testability Evaluation System assign penalties shown for each group and add the total negative points. Record this total on the Score Sheet under N3.

STEP 14

Repeat the STEP 13 procedure for all accessible nodes with 5 or more packages tied together. Record this result on the Score Sheet for N4.

STEP 15

For factors N5 through N9, assign penalties if undesirable design factors are present and enter these in the appropriate places on the Score Sheet. Show 0% if a factor is not a problem to indicate that each factor was considered.

STEP 16

Check each sequential circuit to see if it can be initialized in two ways; using the direct set/reset inputs, and using signal input patterns with a clock line. Penalize (per the Evaluation System) in each case where initialization cannot be accomplished in two ways, and enter these under N10.

STEP 17

For factors N11 and N12 assign possible penalties and enter results on Score Sheet.

STEP 18

For N13 start with any sequential circuit (count of 1) and count each sequential stage directly connected to one of its inputs or to one of its outputs. If an output lead from an otherwise unconnected sequential circuit is connected to the clock input of a sequential circuit in the above cluster, it should also be counted. Expand the count in all directions until all signal leads from all circuits in the cluster reach combinational circuits or a PCB input/output lead.

Assess penalties for each cluster of three or more sequential circuits as shown in the Evaluation System. Continue this process until all sequential circuits have been checked. Total up and record the penalty in the Score Sheet.

STEP 19

For factors N14 through N30 assign possible penalties as per the Evaluation System and record the results on the Score Sheet.

STEP 20

Total up all negative percentage points and record the total negative score. Subtract the total negative score from total basic score to obtain the final PCB rating.

4.3.2 Relationship of PCB Rating to Actual Test Difficulty

In order to determine how the final PCB Testability Rating correlates with actual difficulty-to-test, the average rating limits for typical PCBs are presented below:

PCB Rating	Circuit Test Difficulty
+81% to +100%	Very easy
+66% to +80%	Easy
+46% to +65%	Medium/Easy
+31% to +45%	Medium
+11% to +30%	Hard
+1% to +10%	Very Hard
-100% to 0%	Impossible to test without extreme cost penalties

4.4 PCB TESTABILITY EVALUATION SCORING SYSTEM

4.4.1 Basic Factors

B1 - Percent of Nodes Accessible

An accessible wiring node is one which is connected to an external connector pin.

Percent Accessible Nodes	Actual Rating (%)
(a) 91 to 100	(30)
(b) 81 to 90	(27)
(c) 71 to 80	(24)
(d) 61 to 70	(21)
(e) 51 to 60	(18)
(f) 41 to 50	(15)
(g) 31 to 40	(12)
(h) 21 to 30	(8)
(i) 11 to 20	(4)
(j) 0 to 10	(0)

B2 - Proper Documentation

(1) Mandatory Requirements

(a) Schematic/Logic Diagram provided

(b) Parts List provided

(c) Equivalent logic diagrams of all integrated circuit parts

(d) All documents must be legible

(e) Configuration of the Schematic/Assembly Group must be clearly stated.

(2) Basic Items	Actual Rating (%)
(a) Logic diagrams or schematics (of all detailed parts) provided either on overall print or as individual part specs	4
(b) Detailed performance spec with signal I/O tolerances provided	8
(c) Truth table for each digital IC circuit type shown on schematic or on detailed part drawing provided	3
(d) Functional designations should be shown next to each pin number of all logic packages on the schematic	5

	Actual Rating (%)
(e) Power circuits shown in a single location on the schematic and with voltages labeled	3
(f) Schematic shows reference to corresponding assembly print and part number of next higher assembly	2

B3 - Percent of Sequential Circuits

Each integrated circuit package on the schematic is counted as a single sequential or combinational circuit regardless of its individual complexity.

Percent of Sequential Circuits	Actual Rating (%)
(a) < 15%	25
(b) ≥ 15 but < 25	20
(c) ≥ 25 but < 40	10
(d) ≥ 40 but < 50	5
(e) ≥ 50	0

B4 - Complexity Count

The complexity count is made for sequential circuits only. Combinational ICs are ignored. Use the following list to determine the total count for each type of circuit configuration.

	Total Counts
(a) Flip Flop	7
(b) Latch	7
(c) 4-BIT Shift Register	35
(d) Memory Chip	2^n (n = number of inputs)
(e) Microprocessor	1000
(f) VLSI Chip	1000
(g) All other sequential ICs	See Notes 1 and 2

PCB Complexity Count	Actual Rating (%)
(a) Less than 300	20
(b) 301 to 500	16
(c) 501 to 800	12
(d) 801 to 1200	8
(e) 1201 to 1800	4
(f) 1801 and higher	0

Note 1:

For complex IC circuits with sequential sections, add the count of internal combinational gates and inverters to the total based on:

- Gate = number of input leads plus one
- Inverter = 3

Note 2:

Total count for other sequential ICs is determined by summing the counts of each internal gate with the counts of logic types (a) through (e) above

4.4.2 Negative Factors

N1 - Monostable Circuits

Classify each monostable into one of the three categories listed below and assess the appropriate scoring penalties.

Scoring Factors	Actual Rating (%)
(a) Is tested by analog techniques not requiring digital ATG processing	(-1) per instance
(b) Accessible monostable output driving sequential circuits	(-2) per instance
(c) Inaccessible monostable output driving sequential circuits	(-5) per instance

N2 - 2^n Sequential Counters

Multiply the number of IC packages by the number of internal sequential stages. The scoring factor is equal to the product. Stop count when a combinational circuit is reached.

Scoring Factors	Actual Rating (%)
(a) 5 to 10 with monitor lead only	(-2) per instance
(b) 5 to 10 not accessible	(-3) per instance
(c) 10 or more with monitor lead only	(-4 plus (-0.05(N-10)) per instance
(d) 10 or more not accessible	(-5 plus (-0.1 x (N-10)) per instance

N3 - Maximum Number of Function Blocks per Inaccessible Node

Count the number of different function blocks (circuit packages) connected to the same wiring junction (node). This procedure pinpoints areas of the circuit design where high internal fanouts make fault isolation difficult.

Inaccessible Nodes	Actual Rating (%)
a) 4	(-0.1) per instance
b) 5	(-0.2) per instance
c) 6	(-0.5) per instance
d) 7	(-1.0) per instance
e) 8	(-1.3) per instance
f) 9	(-1.7) per instance
g) 10 and higher	(-2.0) per instance

N4 - Maximum Number of Function Blocks per Accessible Node

Same procedure as N3 but with smaller penalties for high fanout.

Accessible Nodes	Actual Rating (%)
a) 5	(-0.1) per instance
b) 6	(-0.2) per instance
c) 7	(-0.5) per instance
d) 8	(-0.6) per instance
e) 9	(-0.8) per instance
f) 10 and higher	(-1.0) per instance

N5 - Supply Voltage Sequencing Requirements

Two or more supply voltages which require a turn-on and/or turn-off sequence. Assess a -10% penalty for any PCB with this requirement.

N6 - Non-removable Memories (I/O leads accessible)

Any type of memory permanently wired to the PCB with all I/O leads accesible.

Memory Size (BITS)	Actual Rating (%)
a) 100K and over	(-10) per instance
b) 32K to 99K	(-6) per instance
c) 8K to 31K	(-4) per instance
d) 1K to 7K	(-2) per instance

N7 - Non-removable Buried Memory

Any memory permanently wired to the PCB with one or more of its leads not connected to I/O pins.

Memory Size (BITS)	Actual Rating (%)
a) Under 1K	(-5) per instance
b) $\geq$ 1K	(-10) per instance

N8 - Removable Complex Part

If the part is mounted in a socket or the equivalent and must be extracted prior to test access a -1% penalty per instance.

N9 - Non-removable Microprocessor, VLSI Chips or Other Complex Parts

Scoring Factors	Actual Rating (%)
a) All leads accessible to I/O pins	(-3) per instance
b) One or more leads not accessible to I/O pins	(-10) per instance

N10 - Initialization of Sequential Circuits

Sequential circuits should be resetable from an external connector pin (either set or reset) and by applying a digital stimulus of less than 16 patterns to the PCB. Penalties are assessed if either type of reset is absent, and a severe penalty is given for no reset capability.

Scoring Factors	Actual Rating (%)
a) Direct set and <16 pattern reset	No penalty
b) Direct set but no pattern reset	(-0.05) per instance
c) No direct set but <16 pattern reset	(-0.1) per instance
d) No direct set and ≥ 16 pattern reset	(-2) per instance

N11 - External Loading Required

Components which must be added to the ID to perform test (e.g., pullup resistors).

Scoring Factors	Actual Rating (%)
a) 10 resistive loads	(-2)
b) 50 and over resistive load	(-3)
c) > 5 Reactive Loads	(-5)

N12 - Diversity of IC Type Numbers

Scoring Factors	Actual Rating (%)
a) 7 types	No Penalty
b) 10 types	(-1)
c) > 10 types	(-1) for each additional 3 types

N13 - Buried Sequential Logic

Do not count 2^n buried counters under this step.

Scoring Factors	Actual Rating (%)
a) Cluster of 3 or 4 sequential circuits	(-0.1)
b) Cluster ≥ 5	-0.2 [1+ (N-5)] per instance

N14 - Input - Output Pins Distinguished on Schematic

This makes tracing of signal paths easier.

Scoring Factor	Actual Rating (%)
a) Direction arrows not different for input pins versus output pins	(-3)

N15 - Excess Warm-up Time

Time required to stabilize card should not exceed 3 minutes.

Scoring Factor	Actual Rating (%)
a) Over 3 minutes	(-3)

N16 - Tolerance (Perform if information on test equipment is known)

Scoring Factors	Actual Rating (%)
a) Measurement capability at least 10 times more accurate than PCB requirement	No penalty
b) Measurement capability 3 times more accurate than PCB requirement	(-2) per instance
c) Measurement capability less than 3 times more accurate than PCB requirement	(-5) per instance

N17 - High Power

Scoring Factor	Actual Rating (%)
a) More than 5 amps of current required	(-5) per instance
b) High voltage >300Vpp	(-2) per instance
c) Multiple parallel pins for high current	(-1) per instance

N18 - Frequency Critical

Scoring Factor	Actual Rating (%)
a) Requires co-ax in ID	(-5)
b) Over 10 MHz	(-3)
c) Over 4 MHz	(-2)
d) Over 1 MHz	(-1)

N19 - Clock Lines

Scoring Factor	Actual Rating (%)
a) One, externally controlled	(-1)
b) Multiphase, externally controlled	(-2)
c) Single clock, monitor only	(-3)
d) Multiple clocks, monitor only	(-5)
e) Inaccessible free-running clock	(-20)

N20 - External Test Equipment

Test equipment other than that contained in the automatic test equipment.

Scoring Factor	Actual Rating (%)
a) 2 Power supplies or more	(-2)
b) Oscillosope	(-2)
c) Function Generator	(-4)

N21 - Environmental

Special chambers or areas required to perform test.

Scoring Factors	Actual Rating (%)
a) Forced air, ambient or chilled	(-2)
b) Heat, altitude, EMI (chamber)	(-10)

N22 - Adjustments

Trimpots, variable caps, etc.

Scoring Factor	Actual Rating (%)
a) per instance	(-2)
b) per interactive adjustment	(-4)

N23 - Complex Signal Inputs/Outputs

Signals where interpretation by the test operator is required where complex or non-periodic waveshapes are used.

Scoring Factor	Actual Rating (%)
a) 2 coincident unusual wave forms	(-5 per instance)
b) 1 unusual wave form	(-2 per instance)

N24 - Redundant Logic

Logic which because of being in parallel prevents fault isolation and/or detection of individual logic failures. No penalty if built-in-test permits fault isolation of redundant elements.

Scoring Factor	Actual Rating (%)
a) 2 parallel logic functions - inseparable	(-2) per instance
b) 3 and over parallel logic functions - inseparable	(-3) per instance

N25 - Number of Logic Voltages

Scoring Factor	Actual Rating (%)
a) 4	No Penalty
b) > 4	(-1 per logic voltage)

N26 - Number of Power Supplies

Number of separate power supplies which must be supplied by the test station.

Scoring Factors	Actual Rating (%)
a) 3	No penalty
b) > 3	(-1 each additional supply)

N27 - Connectives for Schematic Diagram

The aim of this factor is to guarantee that the schematic/logic diagrams do not impose hardship on the test design engineer.

Scoring Factors	Actual Rating (%)
a) Schematic on single page	No penalty
b) If schematic on multiple pages with connecting leads between pages - then all interpage connectives are numbered showing other page numbers and zones	No penalty
c) If neither a) or b) conditions are met	(-20)

N28 - I/O Pins on Schematic

I/O pins located in the center of prints cause extra work for test designer.

Scoring Factor	Actual Rating (%)
a) All I/O pins not brought to edges of schematic diagram or to a common dotted line	(-5)

N29 - Dual I/O Pin Designation

Scoring Factor	Actual Rating (%)
a) If dual designation of an I/O pin is in different areas of print with no cross reference	(-3) per instance

N30 - Logic Symbols on Schematic

Only a single symbol should be used to describe a specific hardware part. Multiple symbols for identical parts make it difficult to check ATG bit propagation and to design key manual patterns to supplement tests.

Scoring Factor	Actual Rating (%)
a) IC Logic Symbols used are not identical to detail part drawing symbols	(-5)

5 - COST EFFECTIVENESS CONSIDERATIONS

A variety of cost factors were analyzed to determine how to limit test design costs by proper testability design. When a PCB is designed with testability in mind, this will lower overall life cycle costs. Examination of many PCBs during this study has shown that less than 5% were designed for testability. Over half of the PCBs examined showed obvious deficiencies serious enough to cause large and unnecessary expenses for test development.

The results of testability analysis can be productive only if corrective design practices are implemented at the right time; not after equipments have been committed to production or delivered to field sites. Costs can be saved when design corrections precede test program set development. However, testability design requirements should not prematurely control the PCB designer while he is in the process of getting a circuit to function for the first time.

The use of a testability design review checklist and guide showing how to correct specific defects in a PCB is the most economical way to produce testable circuits. When good testability is built into a design it leads to several cost reductions. First, planning estimates for developing test program sets will be far more accurate than was previously possible. These estimates will be lower than before since the hidden roadblocks to successful test integration will have either been eliminated or at least properly identified.

Next, production test costs will be lowered. Product sell-off testing can become very expensive when the equipment is designed without testability. The testability design correction procedure identifies areas of the design which are difficult to access, have high ambiguity factors, or which lack test points.

Once the equipment is deployed, cost savings are realized at field repair sites. Fewer part replacements are made for each repair, less time is required to isolate a fault, and test time is reduced.

A true assessment of the magnitude of cost savings resulting from PCB testability is difficult because existing data does not specifically recognize testability.

Interviews with experienced engineering group leaders led to an apportionment of test design costs. For units integrated on AN/USM-429 test stations, the design and integration portions of test set development normally represented about 70% of the total effort.

In theory, the application of testability design principles prior to test development will make a hard-to-test circuit into a medium-easy circuit with corresponding reduction of test design hours. For a typical PCB test design on the AN/USM-429 requiring 1000 total manhours, about 700 would be expended on design and integration. Application of design-for-testability requirements to such a PCB would probably reduce design and integration time to about 400 manhours with a saving of 300 manhours.

5.1 INCREMENTAL LIFE CYCLE COST TRADEOFFS

Use of an incremental change model for testability life cycle cost tradeoffs was investigated to see if it would lead to meaningful cost comparisons. It was determined that little, if any, real data existed either in government or industry files to substantiate a legitimate cost tradeoff. Too many grouped or extraneous cost factors were present which obscured detailed cost data on individual PCBs. In order to perform life cycle cost studies on PCBs, it is first necessary to have applied a testability redesign process to a large sample of boards dispersed to field sites. Since this has not occurred to date, no feedback data from the field is possible.

5.2 DESIGN COST FINDINGS

The study proved conclusively that redesign for testability prior to PCB production can reduce test engineering effort. It will reduce test program integration time and fault ambiguity.

For a testable PCB fewer test patterns are required and less time is used to develop the fault signature. For example, our demonstration PCB initially required 4,580 test patterns and 78 seconds to detect 92.92% of all possible faults. After redesign for testability, the same PCB required only 1449 test patterns and 28 seconds to detect 100% of all possible faults.

The cost savings investigations made during the study produced limited success in defining specific cost saving areas. What was determined, however, was that true cost savings related to testability are interrelated to many other factors. Accounting practices, types of Automatic Test Equipment (ATE) used, system configurations, spares, and most other integrated logistic support factors dramatically affect cost savings resultant from testability redesign.

A better understanding of how good testability design can help is shown in Figure 5-1. This figure represents the cost to develop a test program set versus the percent of faults detectable for a typical PCB. Consider three different situations represented by the curves.

In the first case, if only 90% of faults are required to be detected, the cost saving of redesigning a PCB for testability would be negligible. In the second case, if 94% of all possible faults must be detected there is a large cost saving. In the third case, where 96 to 100% fault detection is required, the PCB cannot meet the specification without testability redesign. The testable version can achieve 100% fault detection without a significant cost penalty.

The curves plotted in the figure are characteristic for circuits where the technology is close to the state-of-the-art. For older, simpler PCBs, using the most advanced ATE and ATGs, fault detection will approach 98 to 100% without extensive PCB testability redesign. Most new electronic systems use the latest IC technology available which makes good testability design extremely important.

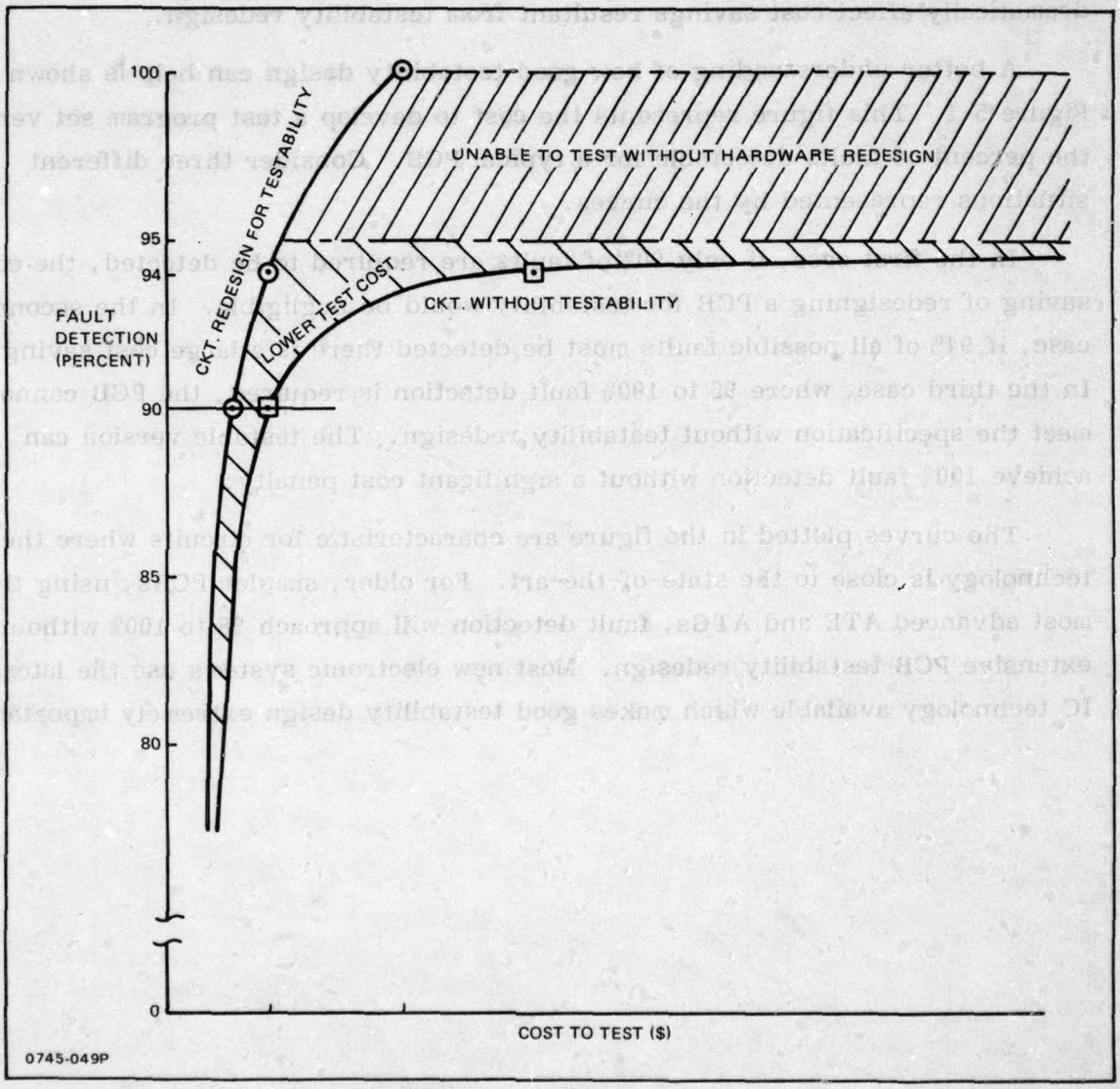


Figure 5-1 Testability Cost Savings

6 - TESTABILITY DEMONSTRATION

6.1 SELECTION OF PCB DEMONSTRATION CIRCUIT

Several considerations influenced the choice of a PCB for use in demonstrating testability. First, the PCB had to provide an opportunity for testability redesign. Second, the circuit had to be representative of current IC technology. Third, the PCB had to physically be available and able to be extensively modified. Finally, the PCB had to be capable of being tested on commercially available ATE. The chosen circuit contained 30 integrated circuits with a high percentage of sequential logic. These stages were connected into three and four stage-buried feedback loops, a shift register which shifted data bits into inverted stages and summed all the Q and $\bar{Q}$ outputs in a common AND gate, a flip/flop which would only pulse for a logic input combination which left it in an unknown logic state, built-in digital hardware race conditions for two phases of a clock derived from a common input pin, and a digital race into an exclusive OR gate driving a latch. These problems made the chosen circuit the most difficult of those surveyed, and made it a real challenge for testability redesign. This circuit is shown in Figures 6-1, 6-2 and 6-3.

6.2 EVALUATION OF UNMODIFIED PCB

An evaluation of the unmodified PCB using the Testability Evaluation System was performed with the results shown in Figure 6-4. The overall score of -27.9% was the lowest for any of the PCBs rated. A key factor in the low score was that none of the 30 sequential circuits could be properly reset.

6.3 REDESIGN FOR TESTABILITY

Using the data from Figure 6-4, a redesign was accomplished which reduced the negative score factors from -76.9% to only -0.1%. The same redesign also raised the basic score from +47% to +58% which made the new overall testability score +59.9% (medium to easy). The number of I/O pins were increased, the percent of nodes accessible was greatly improved, access to interim stages of the shift register section was improved, and all sequential circuits were given means for initialization.

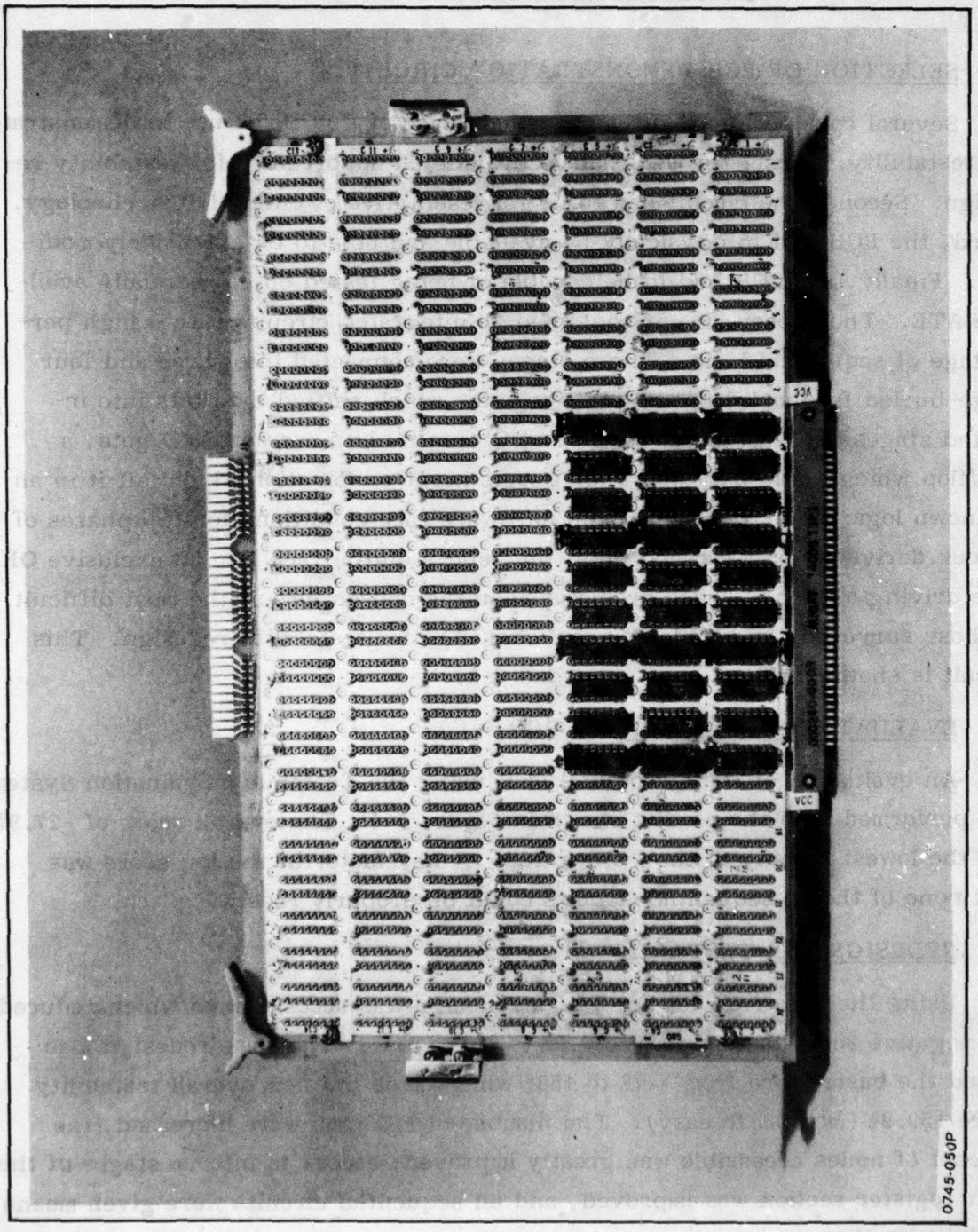
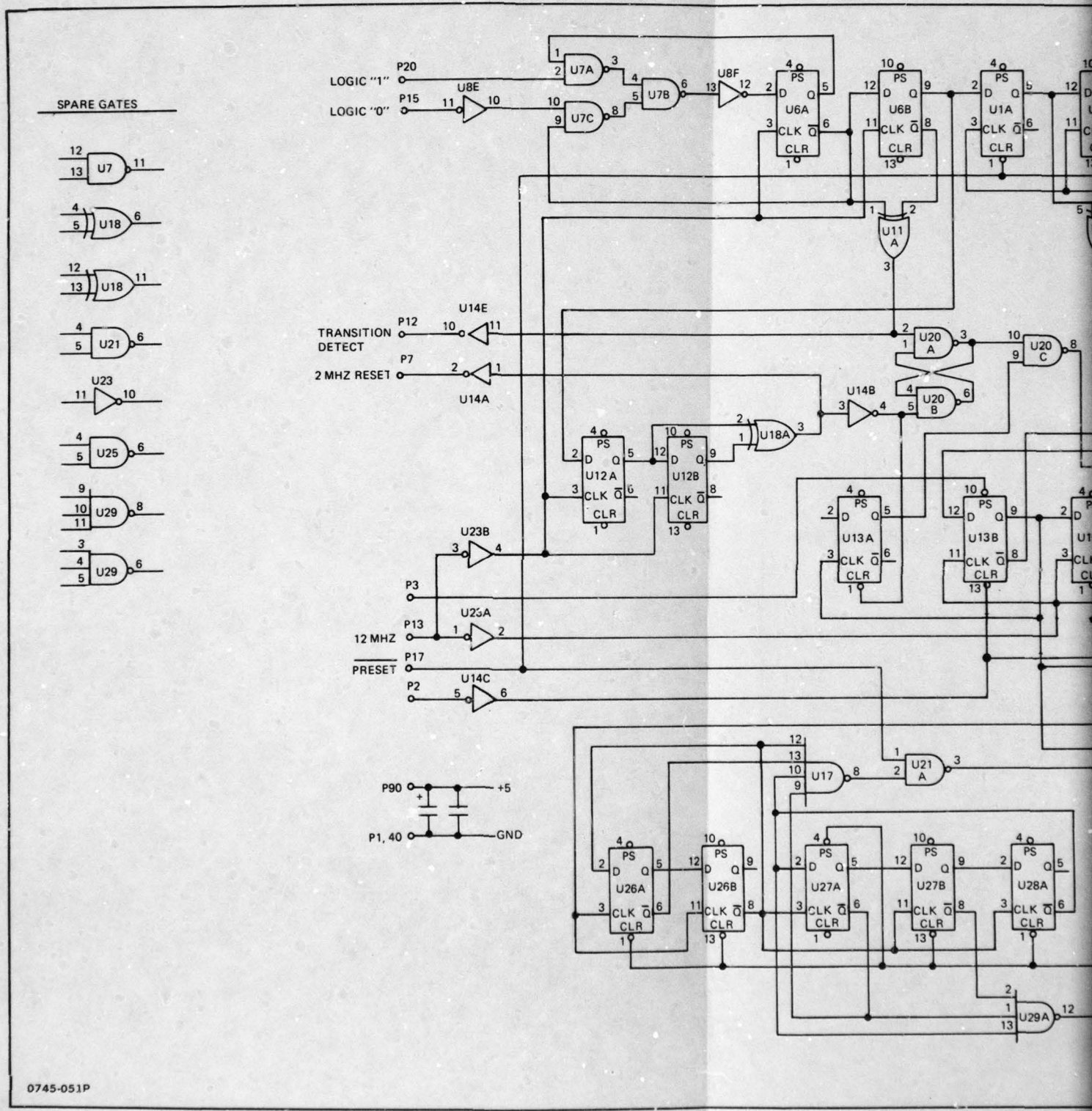


Figure 6-1 Component View of Demonstration Circuit


SPARE GATES
U7
U18
U18
U21
U23
U25
U29
U29
LOGIC "1"
LOGIC "0"
P20
P15
U8E
U7A
U7B
U7C
U8F
U6A
U6B
U1A
U11 A
TRANSITION DETECT
2 MHZ RESET
P12
P7
U14E
U14A
U20 A
U20 C
U20 B
U14B
U18A
U12 A
U12B
U13A
U13B
U23B
U23A
P3
P13
12 MHZ
PRESET
P17
P2
U14C
P90
+5
P1, 40
GND
U17
U21 A
U26A
U26B
U27A
U27B
U28A
U29A
0745-051P

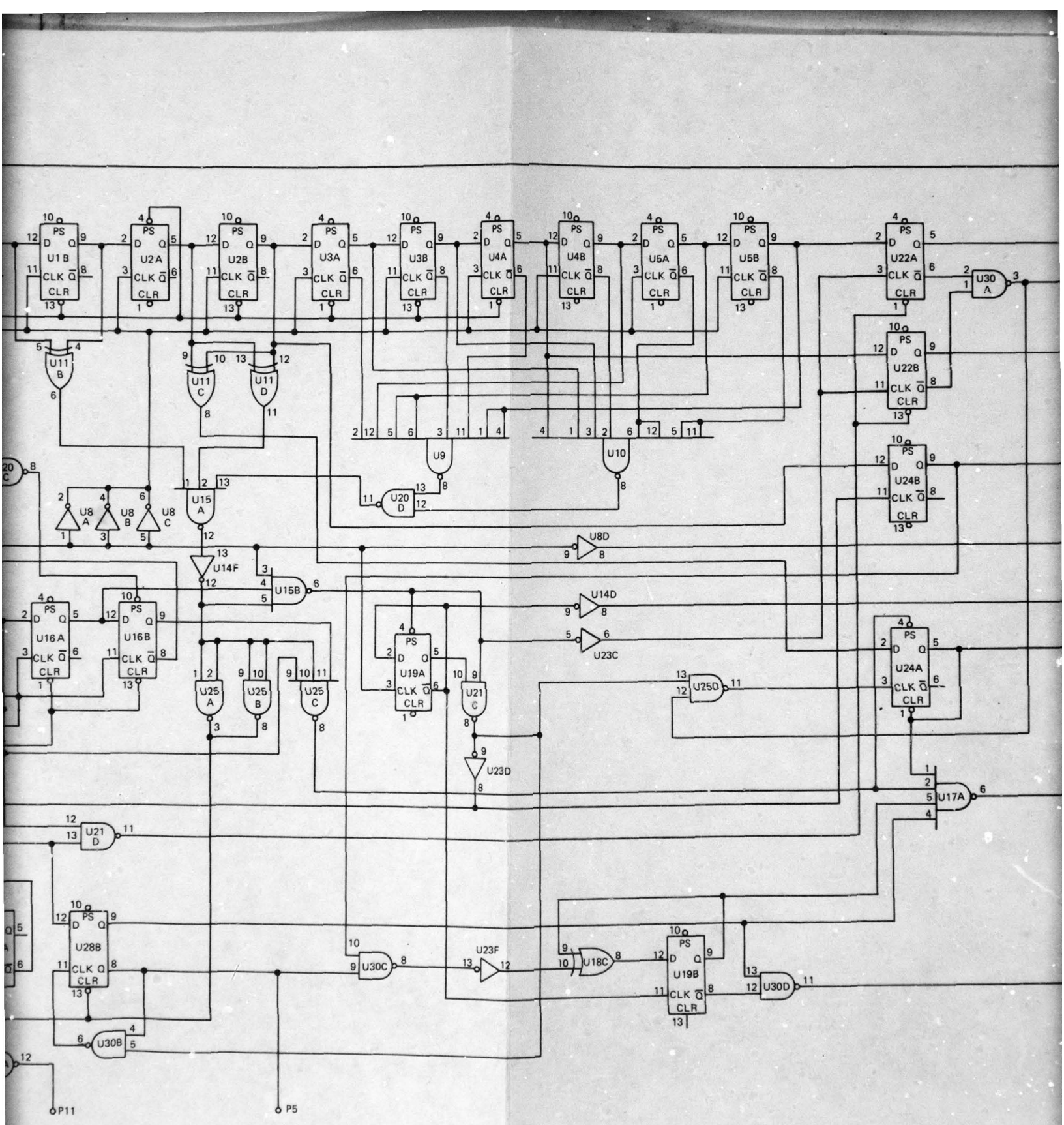

U1B
U2A
U2B
U3A
U3B
U4A
U4B
U5A
U5B
U22A
U22B
U24B
U24A
U11 B
U11 C
U11 D
U9
U10
U30 A
U8 A
U8 B
U8 C
U15 A
U20 D
U8D
U14F
U15B
U14D
U23C
U16A
U16B
U19A
U25 A
U25 B
U25 C
U21 C
U25D
U23D
U17A
U21 D
U28B
U30C
U23F
U18C
U19B
U30D
U30B
P11
P5

Figure 6-2

AD-A082 329 GRUMMAN AEROSPACE CORP BETHPAGE NY F/G 9/1
AN OBJECTIVE PRINTED CIRCUIT BOARD TESTABILITY DESIGN GUIDE AND--ETC(U)
JAN 80 W M CONSOLLA, F G DANNER F30602-78-C-0198

UNCLASSIFIED RADC -TR-79-327 NL

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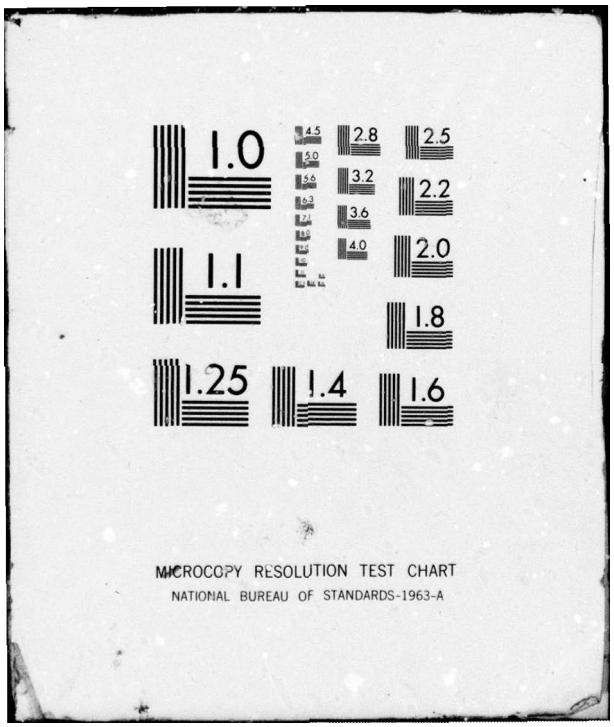

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

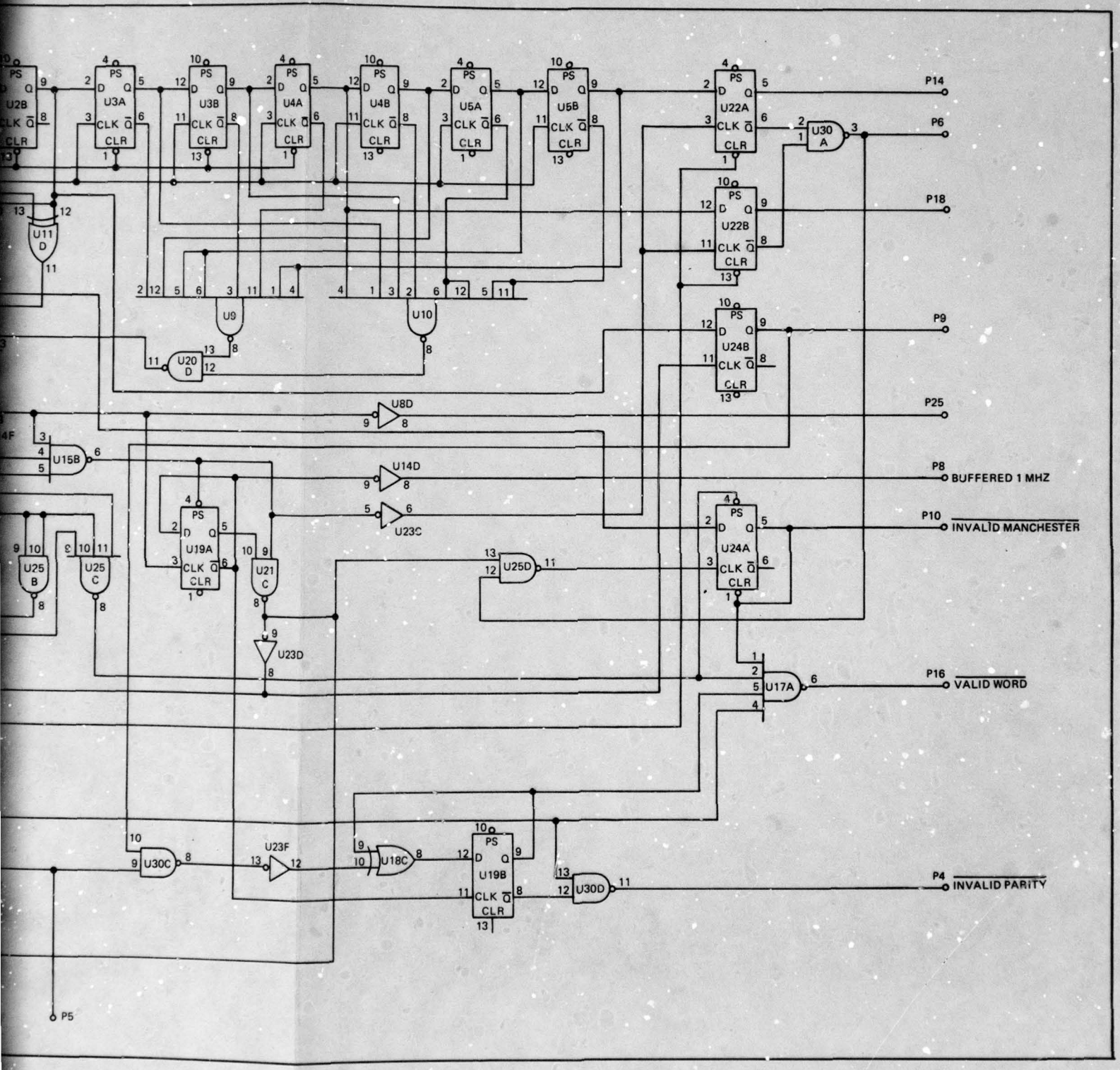
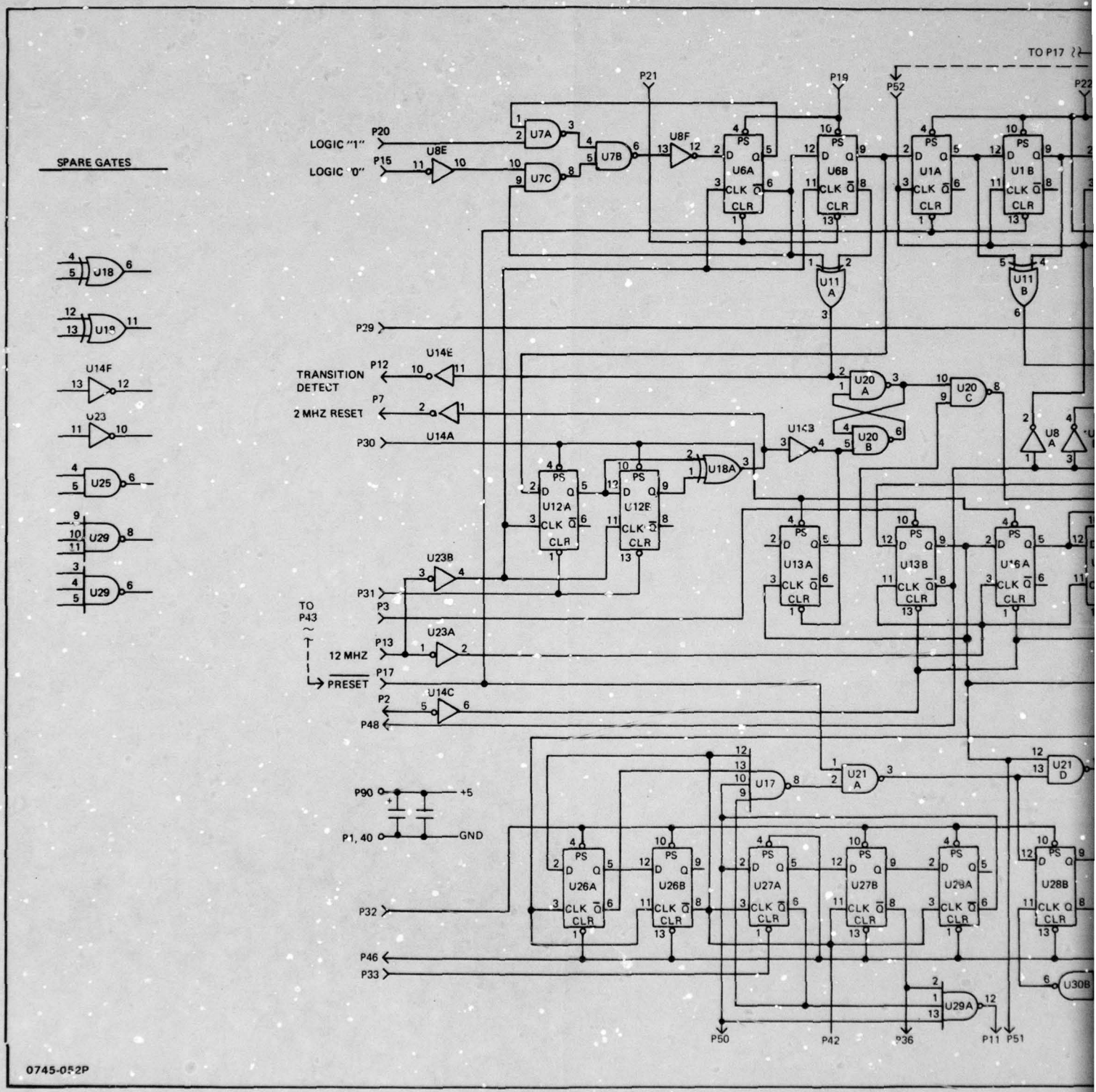


Figure 6-2 Demonstration Circuit Schematic - Original

3


SPARE GATES
U18
U19
U14F
U23
U25
U29
U29
TO P17
P21
P19
P52
P22
P20
LOGIC "1"
P15
LOGIC "0"
U8E
U7A
U7B
U7C
U8F
U6A
U6B
U1A
U1B
U11 A
U11 B
P29
TRANSITION DETECT
P12
U14E
2 MHZ RESET
P7
P30
U14A
U20 A
U20 B
U20 C
U14B
U8 A
U18A
U12A
U12B
U13A
U13B
U16A
U23B
P31
P3
TO P43
12 MHZ
P13
U23A
PRESET
P17
P2
P48
U14C
P90
+5
P1, 40
GND
U17
U21 A
U21 D
U26A
U26B
U27A
U27B
U28A
U28B
U30B
P32
P46
P33
U29A
P50
P42
P36
P11
P51
0745-052P

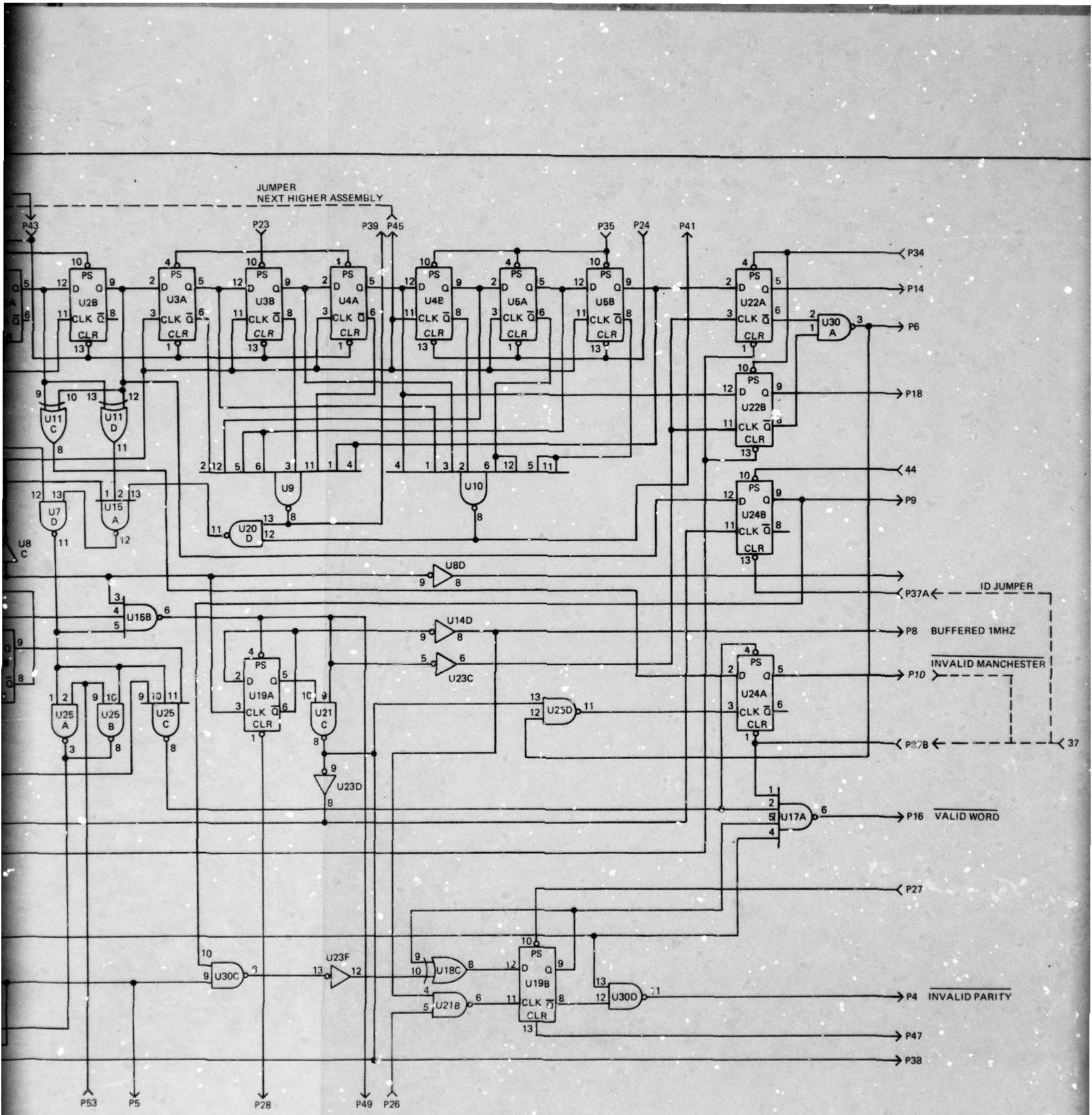


Figure 6-3 Demonstration Circuit Schematic - Revised

FACTOR	DESCRIPTION	SCORE	POSSIBLE RATING(%)	ACTUAL RATING(%)	COMMENTS
A1	PCB Complexity Count	400	10	8	
A2	No. Function Blocks	30	10	10	
A3	No. Counts/Func. Block	13.3	10	4	
A4	I/O Pins	19	10	2	Total Basic Score
A5	I/O Pins per Funct. Block	0.633	10	2	47%
A6	Total Nodes	98	10	10	
A7	Normalized Weighted No. Function Block per Node	2.24	10	6	
A8	% Nodes Accessible	40%	30	5	
B1	Sockets	No		0	Total Positive Score
B2	Uniform Pins	N/A		0	+2%
B3	Labeling	No		0	
B4	Part Access.	OK		+1	
B5	Conformal Coating	No		+1	
C1	Monostable Ckt	0		0	
C2	Counters (Pkgs x Stgs)	91		-13.1	5% + 8.1%
C3	Max. No. Function Blocks / Node (No Access)	2		-0.7	2 + 0.5
C4	Max. No. Function Blocks/ Node (Accessible)	1		-0.1	0.1
C5	Seq. Supply Voltages	No		0	
C6	Non-Remov. Memories	No		0	
C7	Non-Remov. U Processor	No		0	
C8	Init. of Seq. CKTS	All (d's)		-60	30 Flip/Flops
C9	Ext. Loading Req'd.	No		0	
C10	Different Logic Types	7		0	
C11	Buried Seq. Logic	None		0	Same as C2
C12	Max. No. Serial Gates (No Access)	None		0	
C13	Excess Warm-up Time	No		0	Total Negative Score
C14	Tolerance	(a)		0	-76.9%
C15	Non-Defeatable Key Pins	N/A		0	
C16	High Power	No		0	
C17	Critical Frequency	No		0	
C18	Clock Lines	OK		0	
C19	Ext. Test Equipment	No		0	Final Evaluation Score
C20	Environmental	No		0	-27.9%
C21	Adjustments	No		0	
C22	Complex Signal Inputs	No		0	
C23	Redundant Logic	Yes		-3	
C24	No. of Logic Voltages	2		0	
C25	No. of Power Supplies	(a)		0	

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Figure 6-4 Revised PCB Testability Evaluation Score Sheet

A new ATG circuit model of the redesigned PCB was generated. This model greatly reduced the number of test patterns, but did not produce the expected 100% fault detection.

An analysis led to two new conclusions. First, the set-reset leads into several of the sequential circuits were tied in parallel which prevented independent control of the logic states of key flip-flops. This condition made it impossible to propagate desired test patterns into the shift register portion of the PCB. There was a definite need to provide testability redesign features which did more than simply initialize the sequential stages. A change to the leads of the shift register was made to allow patterns to be shifted through the register, and an independently controlled flip/flop stage was set up as a pulse generator; controlled from the inputs to its direct set/reset leads.

Test points were brought out to external pins for the six input summing NAND gates connected to the shift register outputs. Spare gates were used to control two "bottlenecks" in the circuit where signals would be otherwise blocked during fault simulation processing.

A reconvergent fanout condition was discovered which kept the fault detection process in one sector of the circuit from propagating signals to an external output point. A gate was added to gain control of this network and to be able to inject external stimuli. One hundred percent fault detection was achieved using the above redesign strategies.

The Testability Evaluation System and the Test Guide recommendations for redesign were revised to include the above ATG considerations. Most future PCB test programs will be developed by means of automatic test generation. The ability to reach high testability levels will depend heavily on how well the circuit designer can integrate meaningful ATG testability features into the PCB hardware.

6.4 FINAL INTEGRATION & RESULTS

The demonstration PCB, in its original configuration, was tested good on the AN/USM-429 test station (Figure 6-5). This confirmed agreement between the PCB software model and the actual hardware logic. The PCB was then modified to the new "testable" configuration, and was retested good on the same station.

Figure 6-5 Demonstration Card on AN/USM-429

6.5 INSERTION OF FAULTS

A variety of faults were inserted to determine how well the original and the testable programs would detect and isolate problem areas. Data from the fault insertion testing is shown in Figure 6-6. The number of tests were considerably reduced for the testable PCB (1449 versus 4580 test patterns), and test time was reduced from 78 to 28 seconds. For every fault inserted isolation to the faulty chip was obtained. This contrasted with fault isolation of the original configuration where, in some cases, incorrect results were obtained, while in other cases, fault isolation included ambiguous groups of several parts.

In summary, the additional 8% fault detection (100% vs. 92%) for the testable PCB was accompanied by a much better fault resolution. Fault isolation was accomplished faster and more accurately, and the added resolution, greatly reduced the fault ambiguity.

FAULT	CONFIGURATION	RUN TIME (MIN)	PRIMARY FAULT	SECONDARY FAULT
No Fault	Original	1:18	Passed "Good"	
	Testable	0:28	Passed "Good"	
U10-3 Open	Original	1:18	Passed "Good"	
	Testable	3:30	U10	None
U17-5 Open	Original	1:18	Passed "Good"	
	Testable	0:35	U17	None
U23-4 Open	Original	30:00	No Answer	
	Testable	10:00	U6	U12 U23
U5-11 Open	Original	1:30	U5	U20, U10, U9
	Testable	1:05	U5	None
U13-4 Open	Original	1:18	Passed "Good"	
	Testable	1:40	U13, U20	None
U13-4 Gnd	Original	15:15	U20	U13
	Testable	6:00	U13	U20
U20-11 Open U15-13 Gnd	Original	15:30	U1	U2, U3, U4, U31
	Testable	2:30	U15	U11, U20, U7
U15-13 Open	Original	5:00	U20	U9, U10, U15
	Testable	4:40	U15	U20

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Figure 6-6 Results of Fault Insertion Tests

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BIBLIOGRAPHY

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APPENDIX A

LIST OF PCBs ANALYZED

LIST OF PRINTED CIRCUIT CARDS AND MODULES
USED TO ANALYZE TESTABILITY FACTORS
FOR AIR FORCE STUDY CONTRACT
MARCH 30,1979

THE FOLLOWING PRINTED CIRCUIT CARDS AND MODULES WERE USED DURING THE DESIGN FOR TESTABILITY STUDY AS SAMPLES TO DEVELOP THE PCB TESTABILITY EVALUATION SYSTEM, AND TO PERFORM CORRELATION STUDIES. THESE CIRCUITS REPRESENT A GOOD CROSS-SECTION OF AVAILABLE TECHNOLOGY AND WERE SELECTED BECAUSE THEY EITHER REPRESENTED A UNIQUE TYPE OF TEST PROBLEM, OR BECAUSE INFORMATION ON HOW HARD THEY ACTUALLY WERE TO TEST AND INTEGRATE WAS AVAILABLE FROM OUR SUPPORT ENGINEERING SECTION.

PART NUMBER	UNIT #	PGM	NAME	ASSY#	CODE
585907-3	CDL	F-14	REPLY CARD	A7	0001
8354291-501	MODULE	M-MAN	MEMORY UNIT,DIG DATA	32	0002
8354321-504	MODULE	M-MAN	MONITOR UNIT LINE FAIL	21	0003
8000894	CSDC	F-14	MDA-4		0004
A51S24156	SPARROW	F-14	POWER DET. MSL		0005
A51S24102	SPARROW	F-14	VIDEO DET. MSL		0006
A51S24166	SPARROW	F-14	FIRE LINE MONITOR		0007
A51S242.5	SPARROW	F-14	BUFFER COMP MSL RLSE		0008
A32S121-1	USM-415	SP PR	TIMING AND REFERENCE		0009
6[illegible]4	HP2100	M.P.	MICROINSTRUCTION DECODER	A3	0010
6[illegible]12	HP2100	M.P.	MICROINSTRUCTION DECODER	A4	0011
6[illegible]1	HP2100	M.P.	ARITHMETIC/LOGIC CARD	A5	0012
A32S4010-1	GCU	F-14	MICROPROCESSOR GUN CONT		0013
755-1405	FCS	F-14	INBOARD STATION SEQ.	A5	0014
2[illegible]3[illegible]	VDIG	F-14	SCAN CONT NO. 3		0015

2[illegible]51[illegible]	VDIG	F-14	SCAN CONT NO. 5		0016
2[illegible]5[illegible]	VDIG	F-14	SCAN CONT NO. 4		0017
2[illegible]064	VDIG	F-14	MULTIPLIER, VDI		0018
2[illegible]036	VDIG	F-14	MODE VDI		0019
2[illegible]32[illegible]	VDIG	F-14	Y REV CTR AND MEM-MUD		0020
5799480[illegible]	ARPS	E-2C	FIRST RAM PAIR	A42	0021
579938[illegible]	ARPS	E-2C	PRF CONTROL	A38	0022
25-7447[illegible]-9	MODULE	M-MAN	CONTROL MONITOR	54	0023
25-7447[illegible]-1[illegible]	MODULE	M-MAN	CONTROL MONITOR	55	0024
617454	PLB	B1	MIU NO.2 DECODER		0025
2[illegible]31[illegible]	VDIG	F-14	X REV CTR & X MEM-MUD		0026
2[illegible]0[illegible]	VDIG	F-14	SYMBOL GENERATOR		0027
2[illegible]11[illegible]	VDIG	F-14	HEADING GENERATOR		0028

APPENDIX B

TESTABILITY EVALUATION DATA

TYPICAL TESTABILITY EVALUATION DATA FOR PCB USING THE FINAL REVISION SCORING SYSTEM

THE FOLLOWING DATA WAS DEVELOPED DURING THE DESIGN FOR TESTABILITY STUDY TO CHECK ACCURACY OF THE PCB TESTABILITY EVALUATION SYSTEM. BASIC SCORING FACTORS B1 THROUGH B4 ARE SHOWN TOGETHER WITH NEGATIVE SCORING FACTORS N1 THROUGH N30 FOR EACH PCB. ACTUAL TEST ENGINEERING EVALUATIONS ARE LISTED IN THE FINAL DATA SET ALONG WITH TOTAL SCORES FOR ALL CARDS EVALUATED. THIS DATA WAS DEVELOPED USING THE STEP BY STEP PROCEDURE DESCRIBED IN THE PCB TESTABILITY GUIDE.

PART NUMBER	B1	PCT.	B2	PCT.	B3	PCT.	B4	PCT.	TOTAL BASIC	CODE	A
8354291-5#1	77	24%	-	25%	50	5%	434	16%	70%	0002	A
8354321-5#4	100	30%	-	25%	27.2	10%	217	20%	85%	0003	A
A5152415#	48.8	15%	-	17%	42	5%	952	8%	45%	0005	A
A5152410#	33.9	12%	-	11%	36	10%	217	20%	53%	0006	A
6#0#4	75.2	24%	-	12%	11	25%	84	20%	81%	0010	A
6#112	66.7	21%	-	12%	9	25%	105	20%	78%	0011	A
6#0#1	45.5	15%	-	12%	38	10%	3146	0%	37%	0012	A
A3254013#1	94.7	30%	-	9%	28	10%	1964	0%	49%	0013	A
755-14#5	48.5	15%	-	14%	16.8	20%	476	16%	65%	0014	A
2#38#	60.1	21%	-	14%	.06	25%	540	12%	72%	0015	A
2#51#	62	21%	-	16%	0	25%	0	20%	82%	0016	A
2#5##	66.6	21%	-	8%	1.3	25%	300	20%	74%	0017	A
2#0#4	62.5	21%	-	8%	35.7	12%	1214	4%	45%	0018	A
2#030	66.5	21%	-	8%	20.2	20%	1014	8%	57%	0019	A
2#320	60.2	27%	-	8%	28.9	10%	1018	8%	53%	0020	A
617454	40	12%	-	14%	50	5%	210	20%	51%	0025	A
2#310	88.4	27%	-	8%	29.5	10%	2418	0%	45%	0026	A

PART NUMBER	N1	PCT.	N2	PCT.	N3	PCT.	N4	PCT.	N5	PCT.	CODE	B
8354291-5#1	NO	-0%	NO	-0%	NO	-0%	NO	-0%	YES	-3%	0002	B
8354321-5#4	NONE	-0%	NONE	-0%	NONE	-0%	2/5	-0.2%	YES	-3%	0003	B
A5152415#	NO	-0%	YES	-2%	2/.6	-2.6%	.2	-0.2%	NO	-0%	0005	B
A5152410#	NO	-0%	NO	-0%	1.7EC	-3.2%	.2 .5	-0.7%	NO	-0%	0006	B
6#0#4	NO	-0%	NO	-0%	3PL	-3.5%	1	-0.1%	NO	-0%	0010	B
6#112	NO	-0%	NO	-0%	5PL	-7.2%	1PL	-0.1%	NO	-0%	0011	B
6#0#1	NO	-0%	NO	-0%	MANY	-19%	2PL	-0.2%	NO	-0%	0012	B
A3254013#1	NO	-0%	OK	-0%	1	-0.1%	28PL	-28.5%	NO	-0%	0013	B
755-14#5	NO	-0%	2PL	-10.4%	2PL	-4.7%	2PL	-0.8%	NO	-0%	0014	B
2#380	NONE	-0%	NONE	-0%	9PL	-19.7%	2P	-0.7%	NO	-0%	0015	B
2#51#	N/A	-0%	N/A	-0%	6P	-9.4%	3P	-1.9%	NO	-0%	0016	B
2#5##	N/A	-0%	N/A	-0%	5P	-7.5%	3P	-1.7%	NO	-0%	0017	B
2#0#4	NO	-0%	3P	-1.2%	6P	-12.9%	1P	-0.2%	NO	-0%	0018	B
2#030	NONE	-0%	OK	-0%	4P	-5.6%	1/6	-0.2%	NO	-0%	0019	B

2[illegible]32[illegible]	NO	=0%	1P	=7%	1P	=1%	2P	=1.4%	NO	=0%	0020	B
617454	NO	=0%	91	=13.1%	2P	=0.7%	1P	=0.1%	NO	=0%	0025	B
20310	NO	=0%	NO	=0%	2/4	=0.2%	14P	=1.3%	NO	=0%	0026	B

PART NUMBER	N6	PCT.	N7	PCT.	N8	PCT.	N9	PCT.	N10	PCT.	CODE	C
8354291-5M1	NO	=0%	NO	=0%	NO	=0%	NO	=0%	OK	=0%	0002	C
8354321-5M4	NO	=0%	NO	=0%	NO	=0%	NO	=0%	4	=0%	0003	C
A51S24156	NO	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0005	C
A51S24162	NO	=0%	NO	=0%	NO	=0%	NO	=0%	1	=0.2%	0006	C
6[illegible]0M4	NO	=0%	NO	=0%	NO	=0%	NO	=0%	YES	=1.2%	0010	C
6M112	NO	=0%	NO	=0%	NO	=0%	NO	=0%	11C	=1.1%	0011	C
6[illegible]0K1	NO	=0%	NO	=0%	NO	=0%	NO	=0%	OK	=0%	0012	C
A32S4[illegible]1[illegible]=1	NO	=0%	N/A	=0%	N/A	=0%	REM	=0%	OK	=0%	0013	C
755-14[illegible]5	NO	=0%	NO	=0%	NO	=0%	NO	=0%	8	=0.5%	0014	C
20380	NO	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0015	C
2[illegible]510	NO	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0016	C
2[illegible]5[illegible]0	NO	=0,	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0017	C
2[illegible]M04	NO	=0%	NO	=0%	NO	=0%	NO	=0%	YES	=10%	0018	C
2[illegible]03M	NO	=0%	NO	=0,	NO	=0%	NO	=0%	9C	=0.9%	0019	C
2[illegible]32M	NO	=0%	NO	=0%	NO	=0%	NO	=0%	YES	=1.2%	0020	C
617454	NO	=0%	NO	=0%	NO	=0%	NO	=0%	30D	=60%	0025	C
2[illegible]31M	NO	=0%	NO	=0%	NO	=0%	NO	=0%	YES	=2.3%	0026	C

PART NUMBER	N11	PCT.	N12	PCT.	N13	PCT.	N14	PCT.	N15	PCT.	CODE	D
8354291-5M1	YES	=3%	6	=0%	NO	=0%	OK	=0%	NO	=0%	0002	D
8354321-5M4	NO	=0%	10	=1%	NO	=0%	YES	=0%	OK	=0%	0003	D
A51S24156	NO	=0%	13	=2%	NO	=0%	OK	=0%	NO	=0%	0005	D
A51S24162	NO	=0%	17	=3%	YES	=3%	NO	=3%	NO	=0%	0006	D
6[illegible]0M4	NO	=0%	22	=7%	NO	=0%	NO	=3%	NO	=0%	0010	D
6M112	NO	=0%	24	=7%	NO	=0%	NO	=3%	NO	=0%	0011	D
6[illegible]0K1	NO	=0%	11	=1%	NO	=0%	NO	=3%	NO	=0%	0012	D
A32S401[illegible]=1	NO	=0%	20	=4%	NO	=0%	NO	=3%	NO	=0%	0013	D
755-14M5	NO	=0%	14	=2%	NO	=0%	OK	=0%	NO	=0%	0014	D
2[illegible]360	NO	=0%	7	=0%	NO	=0%	OK	=0%	NO	=0%	0015	D
2[illegible]51M	NO	=0%	7	=0%	NO	=0%	OK	=0%	OK	=0%	0016	D
2[illegible]5M0	NO	=0%	8	=1.0%	NO	=0%	OK	=0%	NO	=0%	0017	D
2[illegible]M04	NO	=0%	15	=2%	NO	=0%	OK	=0%	NO	=0%	0018	D
2[illegible]030	NO	=0%	13	=2%	NO	=0%	OK	=0%	NO	=0%	0019	D
2[illegible]32M	NO	=0%	14	=2%	YES	=4%	OK	=0%	NO	=0%	0020	D
617454	NO	=0%	7	=0%	NONE	=0%	OK	=0%	NO	=0%	0025	D
20310	NO	=0%	13	=2%	NO	=0%	OK	=0%	NO	=0%	0026	D

PART NUMBER	N16	PCT.	N17	PCT.	N18	PCT.	N19	PCT.	N20	PCT.	CODE	E
8354291-5M1	OK	=0%	NO	=0%	NO	=0%	OK	=0%	NO	=0%	0002	E
8354321-5M4	OK	=0%	YES	=1%	NO	=0%	NO	=0%	NO	=0%	0003	E
A51S24156	NO	=0%	NO	=0%	YES	=1%	C	=3%	NO	=0%	0005	E
A51S24162	A	=0%	NO	=0%	NO	=0%	NONE	=0%	NO	=0%	0006	E
6[illegible]0M4	NO	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0010	E
6M112	NO	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0011	E
6[illegible]0K1	NO	=0%	NO	=0%	NO	=0%	OK	=0%	NO	=0%	0012	E
A32S40[illegible]=1	NO	=0%	NO	=0%	YES	=1%	C	=3%	NO	=0%	0013	E
755-14M5	NO	=0%	NO	=0%	NO	=0%	OK	=0%	NO	=0%	0014	E
2[illegible]380	OK	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0015	E
2[illegible]510	OK	=0%	OK	=0%	NO	=0%	NO	=0%	NO	=0%	0016	E
2[illegible]5[illegible]0	OK	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0017	E
2[illegible]M04	NO	=0%	NO	=0%	NO	=0%	OK	=0%	NO	=0%	0018	E
2[illegible]030	OK	=0%	NO	=0%	NO	=0%	NO	=0%	NO	=0%	0019	E

2[illegible]320	OK	-0%	OK	-0%	OK	-0%	B	-2%	NO	-0%	0020 E
617454	OK	-0%	OK	-0%	OK	-0%	OK	-0%	OK	-0%	0025 E
2[illegible]310	OK	-0%	OK	-0%	OK	-0%	B	-2%	NO	-0%	0026 E

PART NUMBER	N21	PCT.	N22	PCT.	N23	PCT.	N24	PCT.	N25	PCT.	CODE F
8354291-5M1	AIR	-2%	NO	-0%	NO	-0%	NO	-0%	4	-0%	0002 F
8354321-5M4	AIR	-2%	NONE	-0%	YES	-2%	NO	-0%	4	-0%	0003 F
A51S24156	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0005 F
A51S24162	NO	-0%	3PUT	-6%	YES	-2%	NO	-0%	2	-0%	0006 F
6[illegible]4	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0010 F
60112	NO	-0%	NO	-0%	NO	-0%	NONE	-0%	2	-0%	0011 F
6[illegible]1	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0012 F
A32S4[illegible]1-1	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0013 F
755-14[illegible]5	NO	-0%	NO	-0%	NO	-0%	NO	-0%	4	-0%	0014 F
2[illegible]38[illegible]	NO	-0%	NONE	-0%	NO,	-0%	NO	-0%	2	-0%	0015 F
2[illegible]510	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0016 F
2[illegible]5[illegible]	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0017 F
2[illegible]064	NO	-0%	NO	-0%	NO,	-0%	NO	-0%	2	-0%	0018 F
2[illegible]03[illegible]	NO	-0%	NO	-0%	NO	-0%	NO	-0%	4	-0%	0019 F
2032[illegible]	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0020 F
617454	OK	-0%	OK	-0%	OK	-0%	OK	-0%	2	-0%	0025 F
2[illegible]310	NO	-0%	NO	-0%	NO	-0%	NO	-0%	2	-0%	0026 F

PART NUMBER	N26	PCT.	N27	PCT.	N28	PCT.	N29	PCT.	N30	PCT.	CODE G
8354291-5M1	4	-1%	OK	-0%	OK	-0%	NO	-0%	NG	-5%	0002 G
8354321-5M4	3	-0%	OK	-0%	OK	-0%	NO	-0%	OK	-0%	0003 G
A51S24156	1	-0%	YES	-5%	OK	-0%	NO	-0%	OK	-0%	0005 G
A51S24162	1	-0%	OK	-0%	OK	-0%	NO	-0%	OK	-0%	0006 G
6[illegible]4	2	-0%	OK	-0%	OK	-0%	NO	-0%	OK	-0%	0010 G
60112	2	-0%	OK	-0%	OK	-0%	NO	-0%	OK	-0%	0011 G
6[illegible]1	2	-0%	OK	-0%	OK	-0%	NO	-0%	OK	-0%	0012 G
A32S4[illegible]1-1	1	-0%	NG	-20%	OK	-0%	OK	-0%	OK	-0%	0013 G
755-14[illegible]5	3	-0%	OK	-0%	OK	-0%	NO	-0,	3P	-0%	0014 G
2[illegible]38[illegible]	1	-0%	NG	-20%	NG	-5%	OK	-0%	NG	-5%	0015 G
2[illegible]51[illegible]	1	-0%	NG	-20%	NG	-5%	NO	-0%	NG	-5%	0016 G
2[illegible]5[illegible]	1	-0%	C	-20%	YES	-5%	NO	-0%	YES	-5%	0017 G
2[illegible]0[illegible]4	1	-0%	NG	-20%	NG	-5%	OK	-0%	NG	-5%	0018 G
2[illegible]03[illegible]	2	-0%	NG	-20%	NG	-5%	OK	-0%	NG	-5%	0019 G
2[illegible]32[illegible]	1	-0%	NG	-20%	NG	-5,	35	-0%	NG	-5%	0020 G
617454	1	-0%	OK	-0%	OK	-0%	NO	-0%	OK	-0%	0025 G
2[illegible]310	1	-0%	NG	-20%	NG	-5%	OK	-0%	NG	-5%	0026 G

PART NUMBER	ENGR.EVAL TOTAL BASIC	TOTAL NEG.	TOTAL SCORE	CODE H
8354291-5M1	MED-EASY 70%	-14%	+56%	0002 H
8354321-5M4	EASY 85%	-9,2%	+75,8%	0003 H
A51S24156	HARD 45%	-15,8%	+29,2%	0005 H
A51S24162	HARD 53%	-17,9%	+35,1%	0006 H
6[illegible]4	MED-EASY 81%	-14,8%	+66,2%	0010 H
60112	MED-EASY 78%	-18,4%	+59,6%	0011 H
6[illegible]1	V.HARD 37%	-31,2%	+5,8%	0012 H
A32S4[illegible]1-1	V.HARD 49%	-59,6%	-10,6%	0013 H
755-14[illegible]5	MED 65%	-18,4%	+46,6%	0014 H
2[illegible]38[illegible]	EASY-BAD DOC 72%	-50,4%*	+21,6%	0015 H
2[illegible]51[illegible]	EASY-BAD DOC 82%	-41,3%*	+40,7%	0016 H
2[illegible]5[illegible]	EASY-BAD-DOC 74%	-40,3%*	+33,7%	0017 H
2[illegible]064	WORST VDIG 45%	-39,3%*	+6,7%	0018 H
2[illegible]03[illegible]	MED-BAD DOC 57%	-38,7%*	+18,3%	0019 H

20320	V.HARD DOC BAD	53%	-48.6%*	+4.4%	0020 M
617454	WORST	51%	-73.9%	-22.9%	0025 M
20310	HARD-BAD DOC	45%	-37.8%*	+7.2%	0026 M

* BAD DOCUMENTATION WAS NOT REFLECTED IN EVALUATION BY THE TEST ENGINEERS BUT DID CONTRIBUTE TO A LARGE INCREASE IN COST TO TEST. THIS PENALTY WAS REMOVED WHEN MAKING COMPARISONS TO THE STUDY PCB EVALUATION TEST SCORES.

GLOSSARY OF TERMS

GLOSSARY

Ambiguity Group: The number of possible parts of IC packages which could contain a test fault

ATE: Automatic Test Equipment

ATG: Automatic Test Generation

BIT: Built-in Test

Buried Sequential Logic: Sequential circuits which have no signal leads to a primary I/O.

Fan-in: The number of outputs to which a logic gate is wired

Fan-out: The number of inputs to which a logic output is wired

Feedback Loop: A part of a circuit whose input is dependent on its output

Functional Block: A group of discrete components which act as an equivalent of a logic gate

ID: The interconnecting device used to mate the UUT to the ATE

I/O Pin: Input or Output Pin

Interactive Test Generation: Test engineer uses software terminal to make changes or correction to automatically generated digital test patterns.

LASAR: Logic Automated Stimulus and Response

LOGOS: Automatic test generation system developed by Grumman Aeorspace Corporation

LRU: Line Replaceable Unit

LSI: Large Scale Integration (usually the equivalent of 100 or more gates)

Model: A characterization or mapping of a circuit describing the precise functional relation which is used by an automatic test generator to simulate stimulus-response patterns and fault isolation information.

Node: A point common to one or more logic gates or discrete circuit components

Percent Detect: The total nodes in a circuit which can be found to be stuck at "1" or "0" compared to all possible nodes in a circuit.

PCB: Printed Circuit Board

P/O: Primary Output (usually accessible from edge connector)

Race: A case where a sequence of events cannot be predicted reliably due to variable delays in hardware

RU: Removable Unit

SRU: Shop Replaceable Unit

Stuck at "1" (SA1): A logic state which is permanently held at a logic high

Stuck at "0" (SAO): A logic state which is permanently held at a logic "low"

Testability: A measure of a circuit's capability to be checked for faults which may exist

Test Point: A monitor point on a circuit which can be used for test but not necessarily needed for functional use.

TRD: Test Requirement Document

UUT: Unit Under Test

VAST: Versatile Avionic Shop Test (AN/USM-247)

VLSI: Very Large Scale Integration

ZIF Socket: Zero Insertion Force Socket